

## Product Overview

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050 device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps. The NSi1050 provides thermal protection and transmit data dominant time out function.

## Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage  
VDD1: 2.5V to 5.5V  
VDD2: 4.5V to 5.5V
- Bus fault protection of -40V to +40V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 1Mbps
- High CMTI: 100kV/us
- Low loop delay: <200ns
- High system level EMC performance:  
Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:  
-SOW16  
-DUB8

## Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

## Device Information

| Part Number  | Package | Body Size        |
|--------------|---------|------------------|
| NSi1050-DDBR | DUB8    | 9.30mm x6.40mm   |
| NSi1050-DSWR | SOW16   | 10.30mm x 7.50mm |

## Functional Block Diagrams

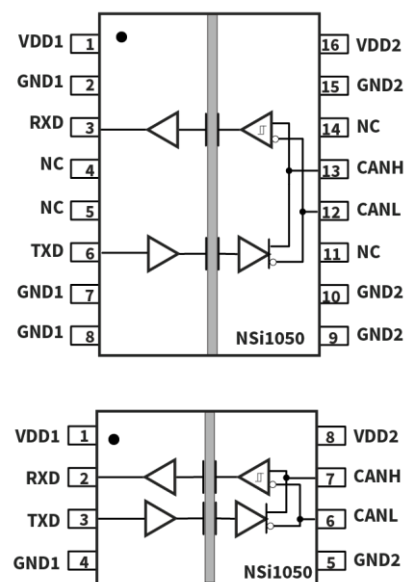


Figure 1. NSi1050 Block Diagram

## INDEX

|  |           |
|--|-----------|
| <b>1. PIN CONFIGURATION AND FUNCTIONS</b> .....        | <b>3</b>  |
| <b>2. ABSOLUTE MAXIMUM RATINGS</b> .....               | <b>5</b>  |
| <b>3. RECOMMENDED OPERATING CONDITIONS</b> .....       | <b>5</b>  |
| <b>4. THERMAL INFORMATION</b> .....                    | <b>5</b>  |
| <b>5. SPECIFICATIONS</b> .....                         | <b>6</b>  |
| 5.1. ELECTRICAL CHARACTERISTICS.....                   | 6         |
| 5.2. SWITCHING ELECTRICAL CHARACTERISTICS .....        | 8         |
| 5.3. PARAMETER MEASUREMENT INFORMATION.....            | 8         |
| <b>6. HIGH VOLTAGE FEATURE DESCRIPTION</b> .....       | <b>12</b> |
| 6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS..... | 12        |
| 6.2. SAFETY-LIMITING VALUES .....                      | 13        |
| 6.3. REGULATORY INFORMATION.....                       | 15        |
| <b>7. FUNCTION DESCRIPTION</b> .....                   | <b>15</b> |
| 7.1. DEVICE FUNCTIONAL MODES .....                     | 15        |
| 7.2. TXD DOMINANT TIME-OUT FUNCTION.....               | 16        |
| 7.3. CURRENT PROTECTION.....                           | 16        |
| 7.4. OVER TEMPERATURE PROTECTION .....                 | 16        |
| <b>8. APPLICATION NOTE</b> .....                       | <b>17</b> |
| 8.1. TYPICAL APPLICATION.....                          | 17        |
| 8.2. PCB LAYOUT.....                                   | 17        |
| <b>9. PACKAGE INFORMATION</b> .....                    | <b>18</b> |
| <b>10. ORDER INFORMATION</b> .....                     | <b>21</b> |
| <b>11. DOCUMENTATION SUPPORT</b> .....                 | <b>21</b> |
| <b>12. TAPE AND REEL INFORMATION</b> .....             | <b>22</b> |
| <b>13. REVISION HISTORY</b> .....                      | <b>24</b> |

### 1. Pin Configuration and Functions

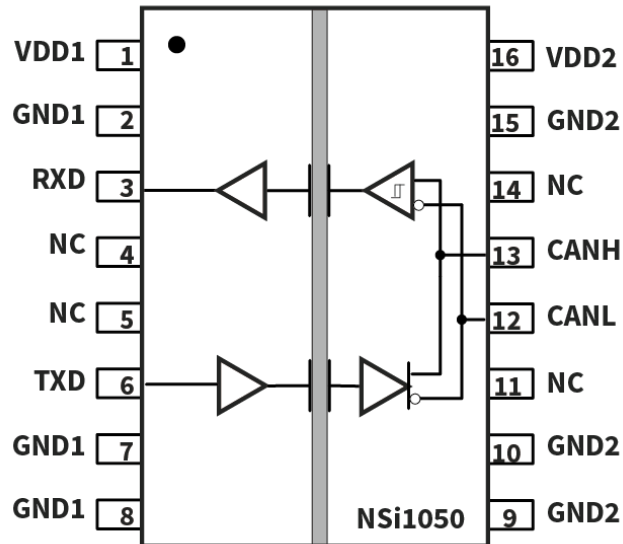


Figure 1.1 NSi1050-DSWR Package

Table1.1 NSi1050-DSWR Pin Configuration and Description

| <b>NSi1050-DSWR<br/>PIN NO.</b> | <b>SYMBOL</b>    | <b>FUNCTION</b>  |
|---------------------------------|------------------|--|
| 1                               | VDD <sub>1</sub> | Power Supply for Side 1  |
| 2                               | GND <sub>1</sub> | Ground 1, the ground reference for Isolator Side 1                           |
| 3                               | RXD              | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| 4                               | NC               | No Connection  |
| 5                               | NC               | No Connection  |
| 6                               | TXD              | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| 7                               | GND <sub>1</sub> | Ground 1, the ground reference for Isolator Side 1                           |
| 8                               | GND <sub>1</sub> | Ground 1, the ground reference for Isolator Side 1                           |
| 9                               | GND <sub>2</sub> | Ground 2, the ground reference for Isolator Bus Side                         |
| 10                              | GND <sub>2</sub> | Ground 2, the ground reference for Isolator Bus Side                         |
| 11                              | NC               | No Connection  |
| 12                              | CANL             | Low-level CAN bus line   |
| 13                              | CANH             | High-level CAN bus line  |
| 14                              | NC               | No Connection  |
| 15                              | GND <sub>2</sub> | Ground 2, the ground reference for Isolator Bus Side                         |
| 16                              | VDD <sub>2</sub> | Power supply for Bus Side  |

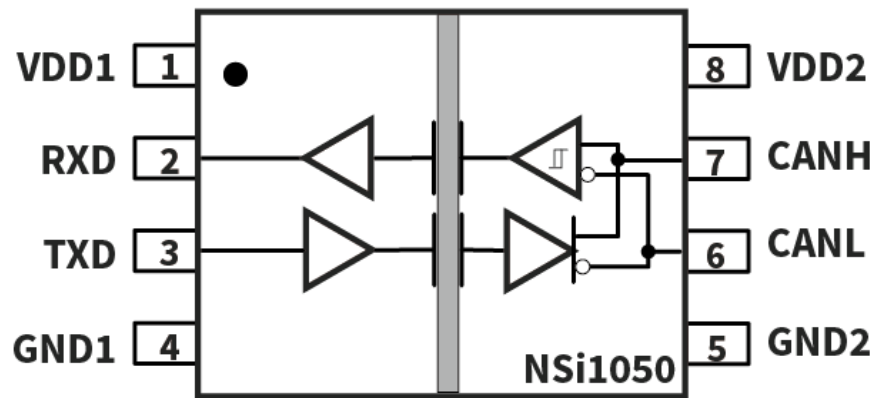


Figure 1.2 NSi1050-DDBR Package

Table1.2 NSi1050-DDBR Pin Configuration and Description

| <b>NSi1050-DDBR<br/>PIN NO.</b> | <b>SYMBOL</b>    | <b>FUNCTION</b>  |
|---------------------------------|------------------|--|
| 1                               | VDD <sub>1</sub> | Power Supply for Side 1  |
| 2                               | RXD              | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| 3                               | TXD              | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| 4                               | GND <sub>1</sub> | Ground 1, the ground reference for Isolator Side 1                           |
| 5                               | GND <sub>2</sub> | Ground 2, the ground reference for Isolator Bus Side                         |
| 6                               | CANL             | Low-level CAN bus line   |
| 7                               | CANH             | High-level CAN bus line  |
| 8                               | VDD <sub>2</sub> | Power supply for Bus Side  |

## 2. Absolute Maximum Ratings

| Parameters              | Symbol                                | Min  | Typ | Max                   | Unit | Comments |
|-------------------------|---------------------------------------|------|-----|-----------------------|------|----------|
| Power Supply Voltage    | VDD <sub>1</sub> , VDD <sub>2</sub>   | -0.5 |     | 6.5                   | V    |          |
| Maximum Input Voltage   | V <sub>TXD</sub>                      | -0.4 |     | VDD <sub>1</sub> +0.4 | V    |          |
| Maximum BUS Pin Voltage | V <sub>CANH</sub> , V <sub>CANL</sub> | -40  |     | +40                   | V    |          |
| Output current          | I <sub>o</sub>                        | -15  |     | 15                    | mA   |          |
| Operating Temperature   | T <sub>opr</sub>                      | -40  |     | 125                   | °C   |          |
| Storage Temperature     | T <sub>stg</sub>                      | -40  |     | 150                   | °C   |          |
| Electrostatic discharge | HBM                                   |      |     | ±6000                 | V    |          |
|                         | CDM                                   |      |     | ±2000                 | V    |          |

## 3. Recommended Operating Conditions

| Parameters   | Symbol                            | Min | Typ | Max  | Unit | Comments |
|--|-----------------------------------|-----|-----|------|------|----------|
| Supply voltage, controller side                    | V <sub>CC1</sub>                  | 2.5 |     | 5.5  | V    |          |
| Supply voltage, bus side                           | V <sub>CC2</sub>                  | 4.5 | 5   | 5.5  | V    |          |
| Voltage at bus pins<br>(separately or common mode) | V <sub>I</sub> or V <sub>IC</sub> | -12 |     | 12   | V    |          |
| High-level input voltage                           | V <sub>IH</sub>                   | 2   |     | 5.25 | V    | TXD      |
| Low-level input voltage                            | V <sub>IL</sub>                   | 0   |     | 0.8  | V    | TXD      |
| High-level output current                          | I <sub>OH</sub>                   | -70 |     |      | mA   | Driver   |
|  |                                   | -4  |     |      | mA   | Receiver |
| Low-level output current                           | I <sub>OL</sub>                   |     |     | 70   | mA   | Driver   |
|  |                                   |     |     | 4    | mA   | Receiver |
| Ambient Temperature                                | T <sub>A</sub>                    | -40 |     | 125  | °C   |          |
| Junction temperature                               | T <sub>J</sub>                    | -40 |     | 150  | °C   |          |

## 4. Thermal Information

| Parameters                               | Symbol                | DUB8 | SOW16 | Unit |
|--|-----------------------|------|-------|------|
| Junction-to-ambient thermal resistance   | θ <sub>JA</sub>       | 73.3 | 76.0  | °C/W |
| Junction-to-case(top) thermal resistance | θ <sub>JC (top)</sub> | 63.2 | 41    |      |
| Junction-to-board thermal resistance     | θ <sub>JB</sub>       | 43.0 | 47.7  |      |

## 5. Specifications

### 5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

| Parameters                              | Symbol              | Min                   | Typ  | Max   | Unit  | Comments   |
|---|---------------------|-----------------------|------|-------|-------|--|
| Supply Voltage                          | VDD <sub>1</sub>    | 2.5                   |      | 5.5   | V     |  |
|   | VDD <sub>2</sub>    | 4.5                   | 5    | 5.5   | V     |  |
| Logic side supply current               | IDD <sub>1</sub>    |                       | 1.97 | 3.00  | mA    | VDD <sub>1</sub> =3.3V, TXD=0                    |
|   |                     |                       | 0.97 | 1.50  | mA    | VDD <sub>1</sub> =3.3V, TXD=VCC1                 |
|   |                     |                       | 2.02 | 3.00  | mA    | VDD <sub>1</sub> =5V, TXD=0                      |
|   |                     |                       | 1.02 | 1.50  | mA    | VDD <sub>1</sub> =5V, TXD=VCC1                   |
| Bus side supply current                 | IDD <sub>2</sub>    |                       | 46   | 70    | mA    | TXD=0V, R <sub>Load</sub> =60Ω                   |
|   |                     |                       | 4.45 | 10    | mA    | TXD=VDD <sub>2</sub>                             |
| Thermal-Shutdown Threshold              | T <sub>TS</sub>     | 155                   | 165  | 180   | °C    |  |
| Common Mode TraNSient Immunity          | CMTI                | ±80                   | ±100 |       | kV/us |  |
| <b>Logic Side</b>                       |                     |                       |      |       |       |  |
| High level input voltage                | V <sub>IH</sub>     | 2                     |      |       | V     | TXD pin  |
| Low level input voltage                 | V <sub>IL</sub>     |                       |      | 0.8   | V     | TXD pin  |
| High level input current                | I <sub>IH</sub>     |                       |      | 10    | uA    | TXD pin  |
| Low level input current                 | I <sub>IL</sub>     | -10                   |      |       | uA    | TXD pin  |
| Output Voltage High                     | V <sub>OH</sub>     | VDD <sub>1</sub> -0.4 |      |       | V     | I <sub>OH</sub> = -4mA, RXD pin                  |
| Output Voltage Low                      | V <sub>OL</sub>     |                       |      | 0.4   | V     | I <sub>OL</sub> = 4mA, RXD pin                   |
| Input Capacitance                       | C <sub>IN</sub>     |                       | 2    |       | pF    | TXD pin  |
| <b>Driver</b>                           |                     |                       |      |       |       |  |
| CANH output voltage (Dominant)          | V <sub>OH(D)</sub>  | 2.8                   | 3.44 | 4     | V     | V <sub>I</sub> =0V, R <sub>Load</sub> =60Ω       |
| CANL output voltage (Dominant)          | V <sub>OL(D)</sub>  | 0.8                   | 1.33 | 2     | V     | V <sub>I</sub> =0V, R <sub>Load</sub> =60Ω       |
| CAN bus output voltage (Recessive)      | V <sub>O(R)</sub>   | 2                     | 2.5  | 3     | V     | TXD=VCC1, R <sub>Load</sub> =60Ω                 |
| Differential output voltage (Dominant)  | V <sub>OD(D)</sub>  | 1.5                   |      | 3     | V     | TXD=0, R <sub>Load</sub> =60Ω                    |
|   |                     | 1                     |      | 3     |       | TXD=0, R <sub>Load</sub> =45Ω                    |
| Differential output voltage (Recessive) | V <sub>OD(R)</sub>  | -0.12                 |      | 0.012 | V     | TXD=VCC1, R <sub>Load</sub> =60Ω, see Figure 2.1 |
|   |                     | -0.5                  |      | 0.05  | V     | TXD=VCC1, NO Load                                |
| Common-mode output voltage              | V <sub>OC</sub>     | 2                     | 2.5  | 3     | V     |  |
| Peak-to-peak Common-mode output voltage | V <sub>OC(PP)</sub> |                       | 250  |       | mV    |  |

| Parameters                                 | Symbol                         | Min  | Typ   | Max | Unit | Comments                              |
|--|--------------------------------|------|-------|-----|------|---------------------------------------|
| Short-circuit output current               | I <sub>OS</sub>                | -105 | -44.1 |     | mA   | CANH=-12V, CANL open, see Figure 5.10 |
|  |                                |      | 0.28  | 1   | mA   | CANH=12V, CANL open, see Figure 5.10  |
|  |                                | -1   | -0.44 |     | mA   | CANL=-12V, CANH open, see Figure 5.10 |
|  |                                |      | 42.5  | 105 | mA   | CANL=12V, CANH open, see Figure 5.10  |
| <b>Receiver</b>                            |                                |      |       |     |      |                                       |
| Positive-going bus input threshold voltage | V <sub>IT+</sub>               |      | 750   | 900 | mV   |                                       |
| Negative-going bus input threshold voltage | V <sub>IT-</sub>               | 500  | 650   |     | mV   |                                       |
| Hysteresis voltage                         | V <sub>HYS</sub>               |      | 100   |     | mV   |                                       |
| Input capacitance to ground                | C <sub>I</sub>                 |      | 13    |     | pF   | CANH or CANL                          |
| Differential input                         | C <sub>ID</sub>                |      | 5     |     | pF   |                                       |
| Differential input resistance              | R <sub>ID</sub>                | 30   |       | 80  | kΩ   |                                       |
| Input resistance                           | R <sub>IN</sub>                | 15   | 30    | 40  | kΩ   |                                       |
| Input resistance matching                  | R <sub>I<sub>match</sub></sub> | -3   |       | +3  | %    | CANH=CANL                             |
| Common-mode voltage range                  | V <sub>COM</sub>               | -12  |       | +12 | V    |                                       |

### 5.2. Switching Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

| Parameters   | Symbol               | Min | Typ | Max | Unit | Comments   |
|--|----------------------|-----|-----|-----|------|--|
| Loop delay1  | T <sub>loop1</sub>   | 100 | 165 | 210 | ns   | Driver input to receiver output, Recessive to Dominant |
| Loop delay2  | T <sub>loop2</sub>   | 80  | 125 | 170 | ns   | Driver input to receiver output, Dominant to Recessive |
| <b>Driver</b>  |                      |     |     |     |      |  |
| Propagation delay time, dominant -to- recessive output | t <sub>PLH</sub>     |     | 53  | 140 | ns   |  |
| Propagation delay time, recessive -to- dominant output | t <sub>PHL</sub>     |     | 78  | 110 | ns   |  |
| Differential output signal rise time                   | t <sub>r</sub>       |     | 42  |     | ns   |  |
| Differential output signal fall time                   | t <sub>f</sub>       |     | 32  |     | ns   |  |
| Bus dominant time-out time                             | t <sub>TXD_DTO</sub> | 300 | 468 | 700 | us   | See Figure 5.9   |
| <b>Receiver</b>  |                      |     |     |     |      |  |
| Propagation delay time, low-to-high-level output       | t <sub>PLH</sub>     | 65  | 80  | 150 | ns   |  |
| Propagation delay time, high-to-low-level output       | t <sub>PHL</sub>     | 80  | 100 | 150 | ns   |  |
| RXD signal rise time                                   | t <sub>r</sub>       |     | 3   |     | ns   |  |
| RXD signal fall time                                   | t <sub>f</sub>       |     | 3   |     | ns   |  |
| Fail-Safe output delay time from bus-side power loss   | t <sub>fs</sub>      |     | 4.2 |     | us   | VDD1=5V  |

### 5.3. Parameter Measurement Information

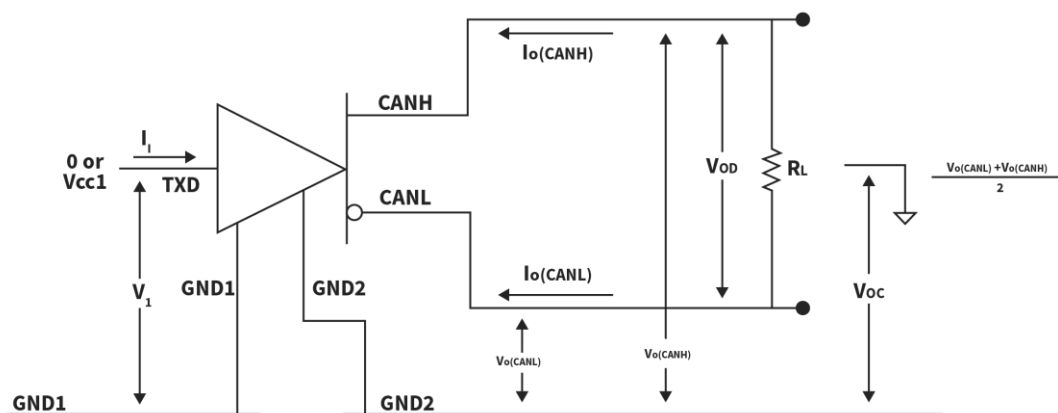


Figure 5.1. Driver Voltage, Current and Test Definitions



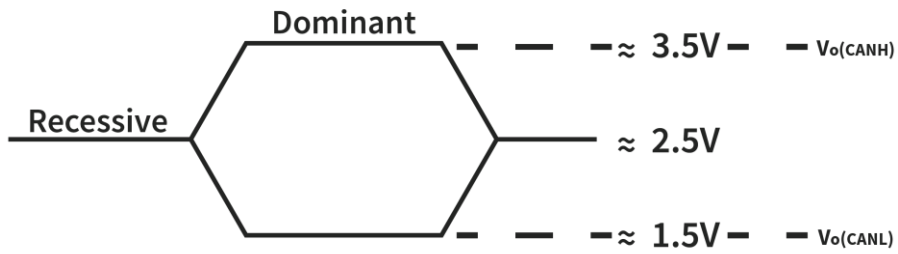


Figure 5.2. Bus Logic State Voltage Definitions

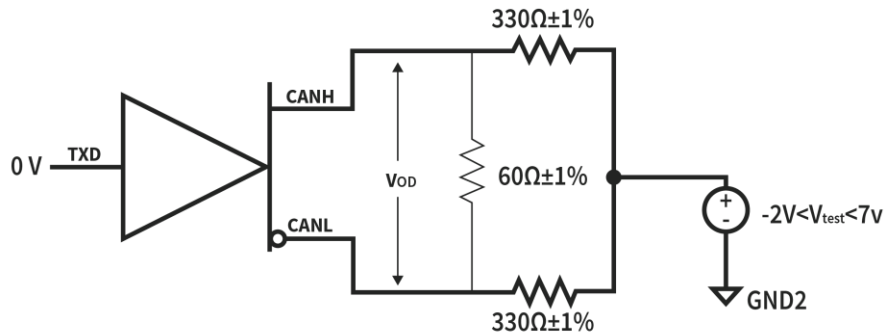
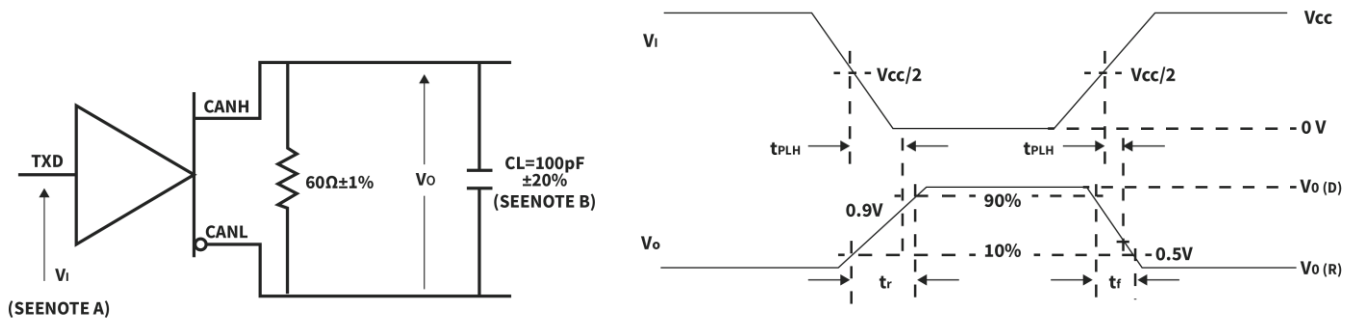


Figure 5.3. Driver VOD With Common-Mode Loading Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.
- B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveform

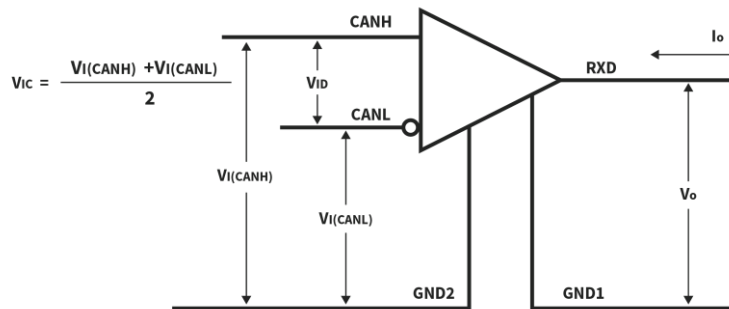
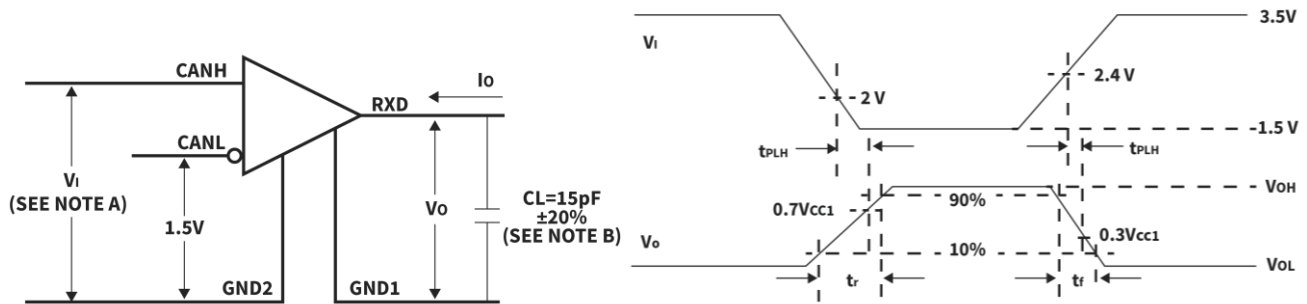


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_o = 50 \Omega$ .  
 B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 5.6. Receiver Test Circuit and Voltage Waveform

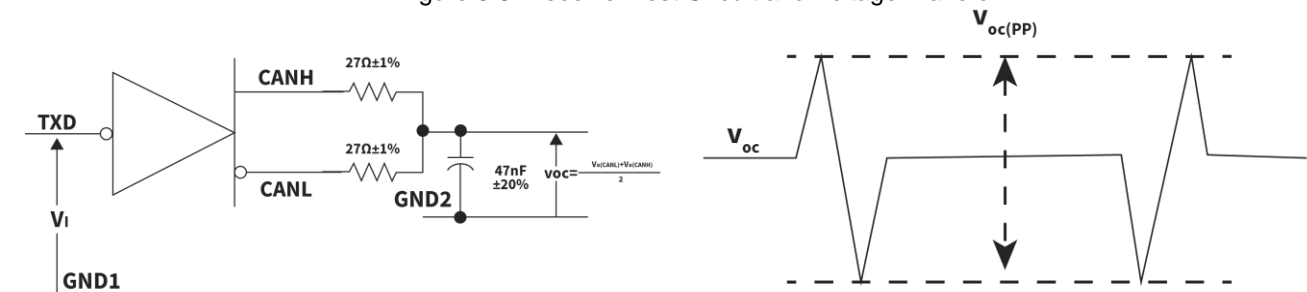


Figure 5.7. Peak-to-Peak Output Voltage Test Circuit and Waveform

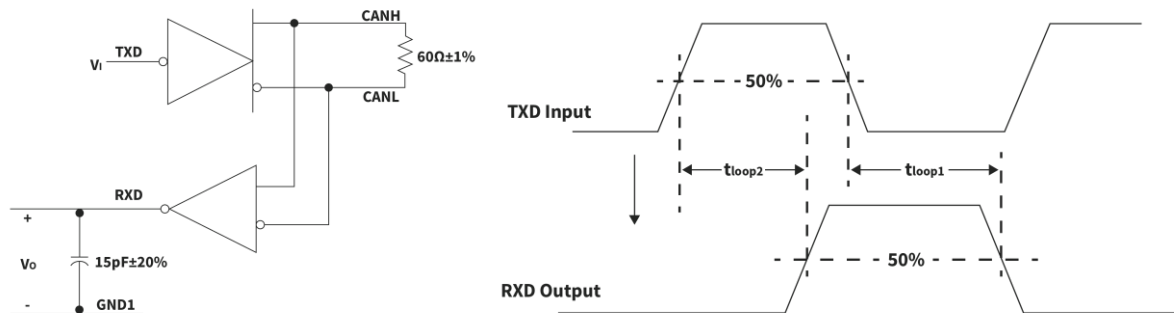
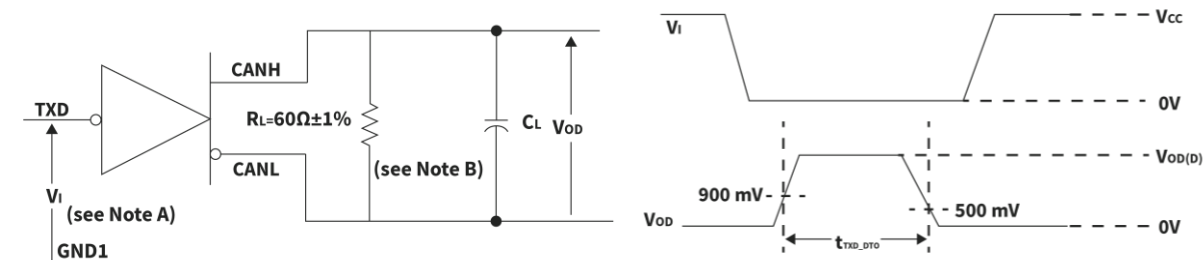


Figure 5.8.  $t_{LOOP}$  Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_o = 50 \Omega$ .  
 B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 5.9. Dominant Time-out Test Circuit and Voltage Waveform

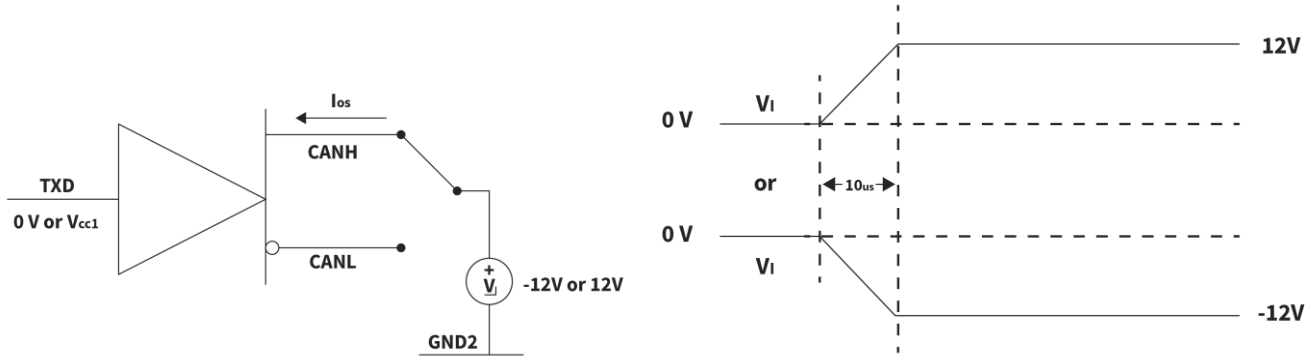


Figure 5.10. Driver Short-Circuit Current Test Circuit and Waveform

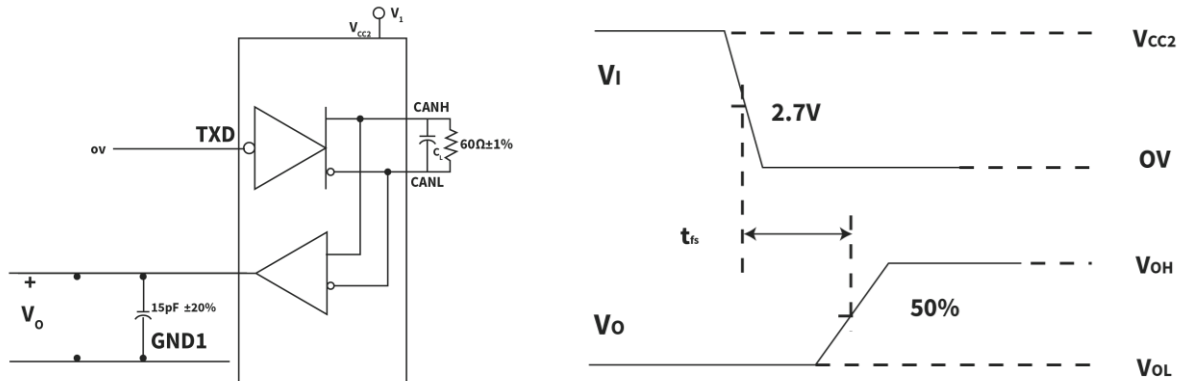


Figure 5.11. Fail-Safe Delay Time Test Circuit and Voltage Waveform

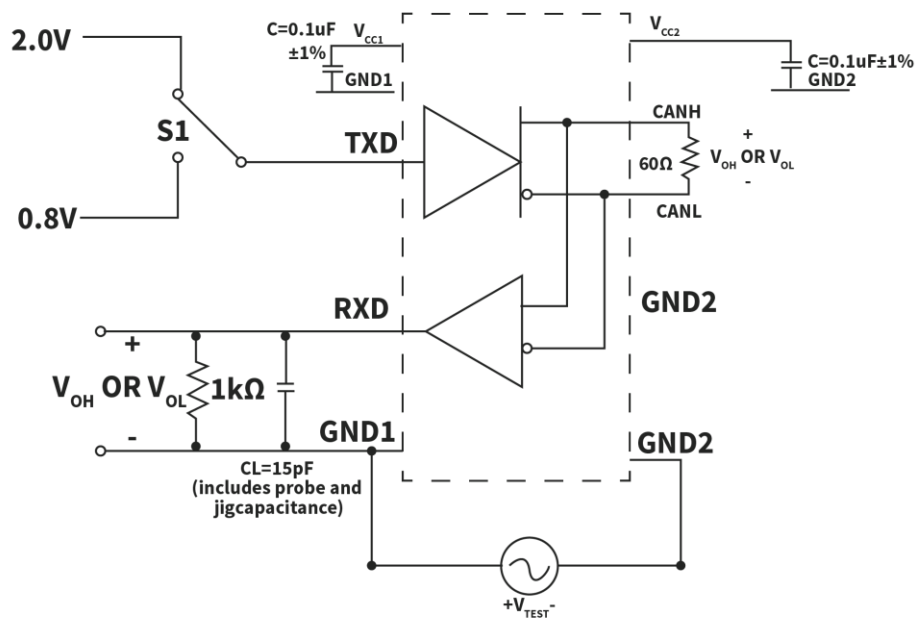


Figure 5.12. Common-Mode Transient Immunity Test Circuit

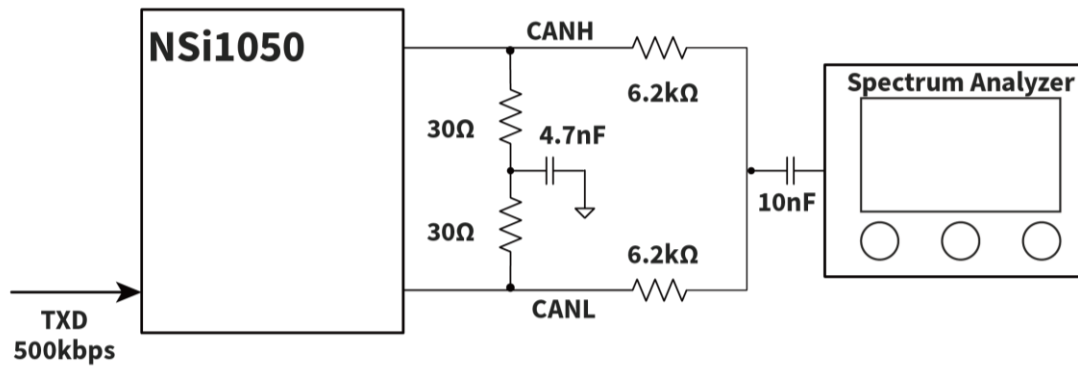


Figure 5.13. Electromagnetic Emissions Measurement Setup

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

| Description  | Test Condition  | Symbol              | Value     |          | Unit              |
|--|---|---------------------|-----------|----------|-------------------|
|  |   |                     | DUB8      | SOW16    |                   |
| Min. External Air Gap (Clearance)                                    |   | CLR                 | 6.5       | 8        | mm                |
| Min. External Tracking (Creepage)                                    |   | CPG                 | 6.5       | 8        | mm                |
| Distance through the Insulation                                      |   | DTI                 | 20        |          | um                |
| Comparative Tracking Index   | DIN EN 60112 (VDE 0303-11)  | CTI                 | >400      | >600     | V                 |
| Material Group   | IEC 60112   |                     | II        | I        |                   |
| Installation Classification per DIN VDE 0110                         |   |                     |           |          |                   |
| For Rated Mains Voltage ≤ 150Vrms                                    |   |                     | I to IV   | I to IV  |                   |
| For Rated Mains Voltage ≤ 300Vrms                                    |   |                     | I to III  | I to IV  |                   |
| For Rated Mains Voltage ≤ 600Vrms                                    |   |                     | I to II   | I to IV  |                   |
| For Rated Mains Voltage ≤ 1000Vrms                                   |   |                     | I         | I to III |                   |
| Insulation Specification per DIN VDE V 0884-11:2017-01 <sup>1)</sup> |   |                     |           |          |                   |
| Climatic Category  |   |                     | 10/105/21 |          |                   |
| Pollution Degree   | per DIN VDE 0110, Table 1   |                     | 2         |          |                   |
| Maximum Working Isolation Voltage                                    | AC voltage  | V <sub>IOWM</sub>   | 400       | 1500     | V <sub>RMS</sub>  |
|  | DC voltage  |                     | 565       | 2121     | V <sub>DC</sub>   |
| Maximum Repetitive Isolation Voltage                                 |   | V <sub>IORM</sub>   | 565       | 2121     | V <sub>peak</sub> |
| Input to Output Test Voltage, Method B1                              | V <sub>ini. b</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.5,<br>t <sub>ini</sub> = t <sub>m</sub> = 1 sec, q <sub>pd</sub> ≤ 5 pC, | V <sub>pd (m)</sub> | 847       | \        | V <sub>peak</sub> |

| Description  | Test Condition   | Symbol      | Value      | Unit |            |
|--|--|-------------|------------|------|------------|
|  | 100% production test   |             |            |      |            |
|  | $V_{ini. b} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.875$ , $t_{ini} = t_m = 1 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$ ,<br>100% production test |             | \          | 3977 |            |
| Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1                         | $V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.3$ ,<br>$t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$      | $V_{pd(m)}$ | 678        | \    | $V_{peak}$ |
|  | $V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.6$ ,<br>$t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$      |             | \          | 3394 |            |
| Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3 | $V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.2$ ,<br>$t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$      | $V_{pd(m)}$ | 678        | 2545 | $V_{peak}$ |
| Maximum Transient Isolation Voltage  | $t = 60 \text{ sec}$   | $V_{IOTM}$  | 5300       | 8000 | $V_{peak}$ |
| Maximum Surge Isolation Voltage  | Test method per IEC62368-1,<br>1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$   | $V_{IOSM}$  | 5384       | \    | $V_{peak}$ |
|  | Test method per IEC62368-1,<br>1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$   |             | \          | 6250 |            |
| Isolation Resistance   | $V_{IO} = 500 \text{ V}$ , $T_{amb} = T_S$   | $R_{IO}$    | $>10^9$    |      | $\Omega$   |
|  | $V_{IO} = 500 \text{ V}$ , $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$   |             | $>10^{11}$ |      | $\Omega$   |
| Isolation Capacitance  | $f = 1\text{MHz}$  | $C_{IO}$    | 1.2        |      | pF         |
| Insulation Specification per UL1577  |  |             |            |      |            |
| Withstand Isolation Voltage  | $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1 \text{ sec}$ ,<br>100% production test  | $V_{ISO}$   | 3000       | 5000 | $V_{rms}$  |

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 6.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi1050-DDBR

| Description           | Test Condition   | Value | Unit |
|-----------------------|--|-------|------|
| Safety Supply Power   | $R_{\theta JA} = 73.3 \text{ }^\circ\text{C/W}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$                     | 1705  | mW   |
| Safety Supply Current | $R_{\theta JA} = 73.3 \text{ }^\circ\text{C/W}$ , $V_I = 5\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | 341   | mA   |

|                                  |  |     |    |
|----------------------------------|--|-----|----|
| Safety Temperature <sup>2)</sup> |  | 150 | °C |
|----------------------------------|--|-----|----|

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of DUB8 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

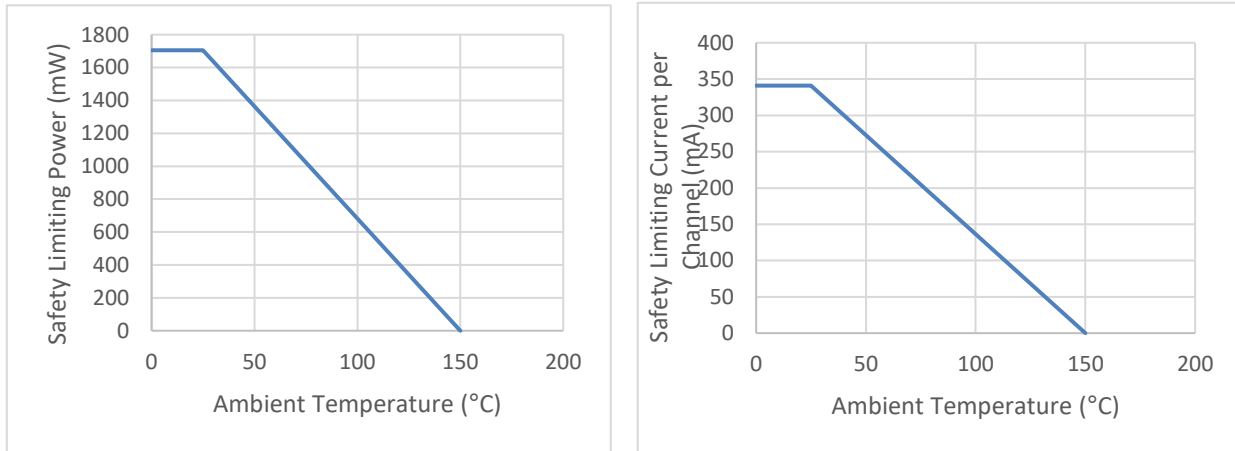


Figure 6.1 NSi1042-DSWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi1050-DSWR

| Description                      | Test Condition   | Value | Unit |
|----------------------------------|--|-------|------|
| Safety Supply Power              | $R_{\theta JA} = 76 \text{ }^\circ\text{C/W}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$                     | 1645  | mW   |
| Safety Supply Current            | $R_{\theta JA} = 76 \text{ }^\circ\text{C/W}$ , $V_I = 5\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | 329   | mA   |
| Safety Temperature <sup>2)</sup> |  | 150   | °C   |

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

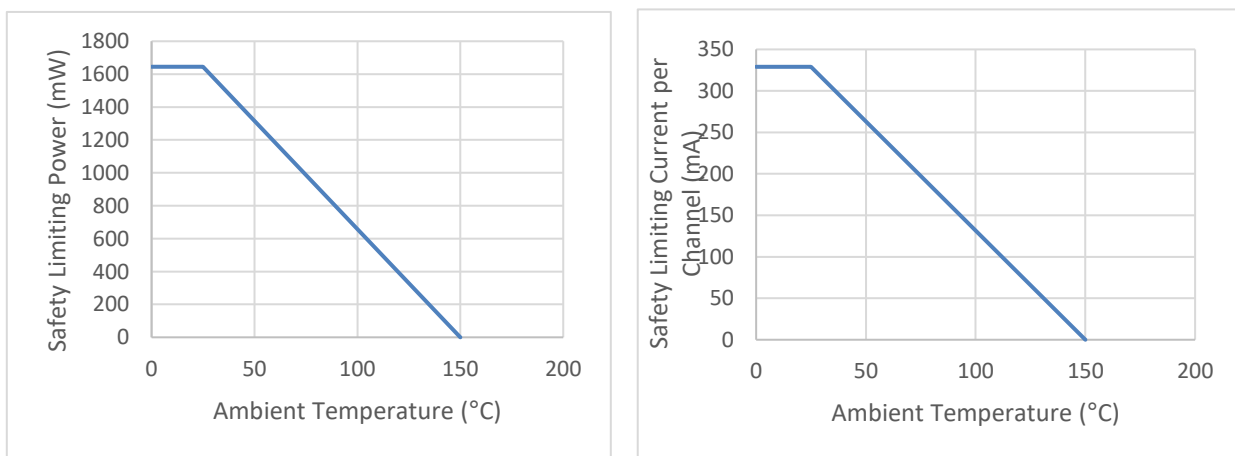


Figure 6.2 NSi1042-DSWR/NSi1052-DSWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. Regulatory information

The NSi1050-DDBR is approved by the organizations listed in table.

|   | <b>CUL</b>  | <b>VDE</b>   | <b>CQC</b>                                   |
|---|---|--|--|
| UL 1577 Component Recognition Program <sup>1</sup>        | Approved under CSA Component Acceptance Notice 5A         | DIN VDE V 0884-11:2017-01 <sup>2</sup>   | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 3000V <sub>rms</sub> Isolation voltage | Single Protection, 3000V <sub>rms</sub> Isolation voltage | Basic Insulation 565V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>peak</sub> | Basic insulation                             |
| File (E500602)  | File (E500602)  | File (40050121)  | File (CQC20001263786)                        |

The NSi1050-DSWR is approved by the organizations listed in table.

|   | <b>CUL</b>  | <b>VDE</b>  | <b>CQC</b>                                   |
|---|---|---|--|
| UL 1577 Component Recognition Program <sup>1</sup>        | Approved under CSA Component Acceptance Notice 5A         | DIN VDE V 0884-11:2017-012  | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 5000V <sub>rms</sub> Isolation voltage | Single Protection, 5000V <sub>rms</sub> Isolation voltage | Reinforced Insulation 2121V <sub>peak</sub> , V <sub>IOSM</sub> =6250 <sub>peak</sub> | Basic insulation                             |
| File (E500602)  | File (E500602)  | File (pending)  | File (CQC20001264939)                        |

## 7. Function Description

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050-DSWR device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while the NSi1050-DDBR device is safety certified by UL1577 support 3kV<sub>rms</sub> insulation withstand voltages. The NSi1050 is providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps. The NSi1050 provides thermal protection and transmit data dominant time out function.

### 7.1. Device Functional Modes

Table 7.1. Driver Function Table

| <b>TXD</b> | <b>CANH</b> | <b>CANL</b> | <b>BUS STATE</b> |
|------------|-------------|-------------|------------------|
| L          | H           | L           | Dominant         |
| H          | Z           | Z           | Recessive        |
| Open       | Z           | Z           | Recessive        |

<sup>1</sup> H= high level; L=low level; Z= common mode(recessive) bias to V<sub>CC</sub>/2

Table 7.2. Receiver Function Table

| <b>V<sub>ID</sub>=CANH-CANL</b> | <b>RXD</b> | <b>BUS STATE</b> |
|---------------------------------|------------|------------------|
| V <sub>ID</sub> ≥ 0.9V          | L          | Dominant         |
| 0.5 < V <sub>ID</sub> < 0.9V    | X          | Uncertain        |
| V <sub>ID</sub> ≤ 0.5V          | H          | Recessive        |
| Open                            | H          | Recessive        |

<sup>1</sup> H= high level; L=low level; X= uncertain

## 7.2. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{TXD\_DTO}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

## 7.3. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

## 7.4. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature  $T_{TS}$ , the output drivers will be disabled until the virtual junction temperature becomes lower than  $T_{TS}$  and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.



## 8. Application Note

### 8.1. Typical Application

The NSi1050 requires a 0.1  $\mu\text{F}$  bypass capacitors between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. The figure5.1 is the basic schematic of NSi1050.

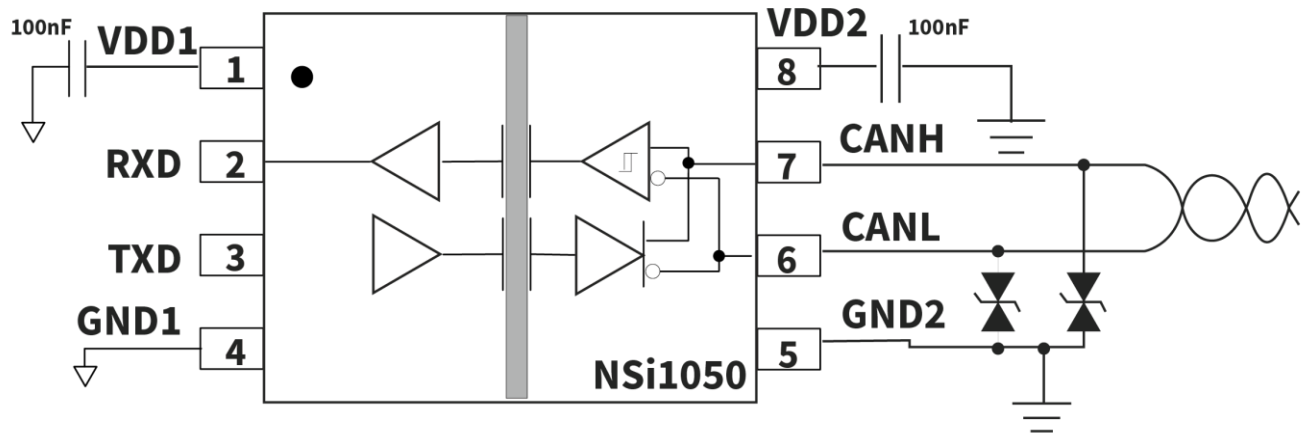


Figure8.1 Basic schematic of NSi1050

### 8.2. PCB Layout

The recommended PCB layout shown below.

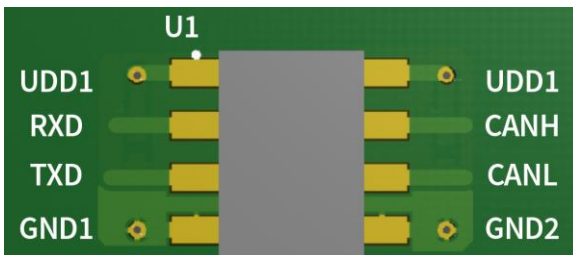


Figure8.2 Recommended PCB Layout — Top Layer Layer



Figure8.3 Recommended PCB Layout — Bottom

### 9. Package Information

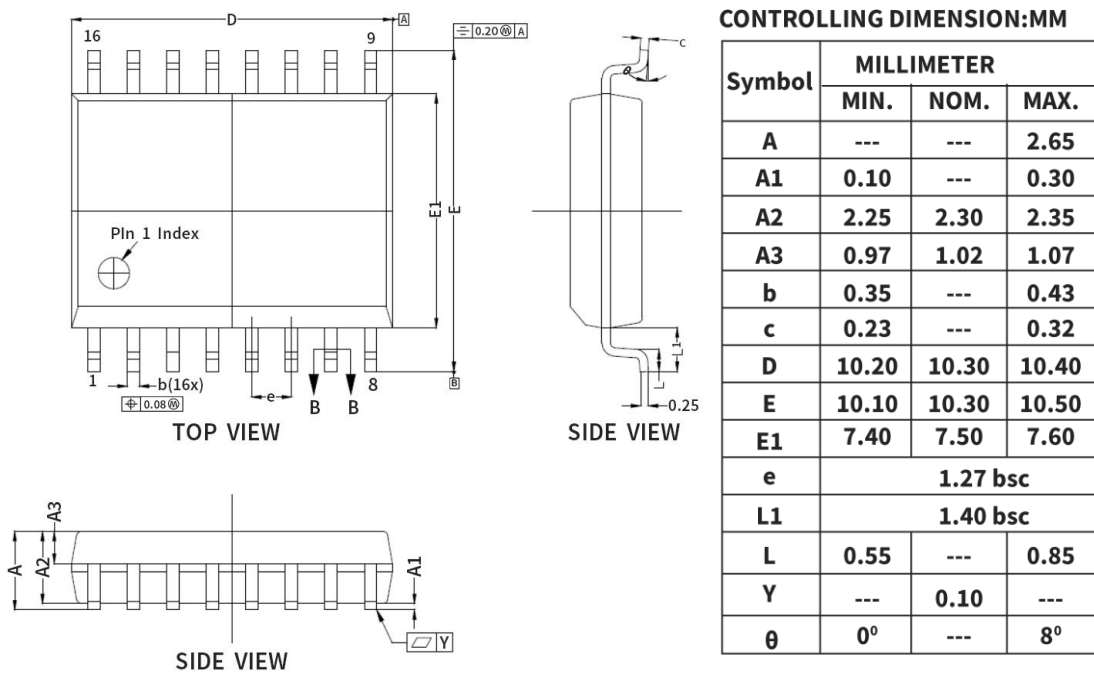
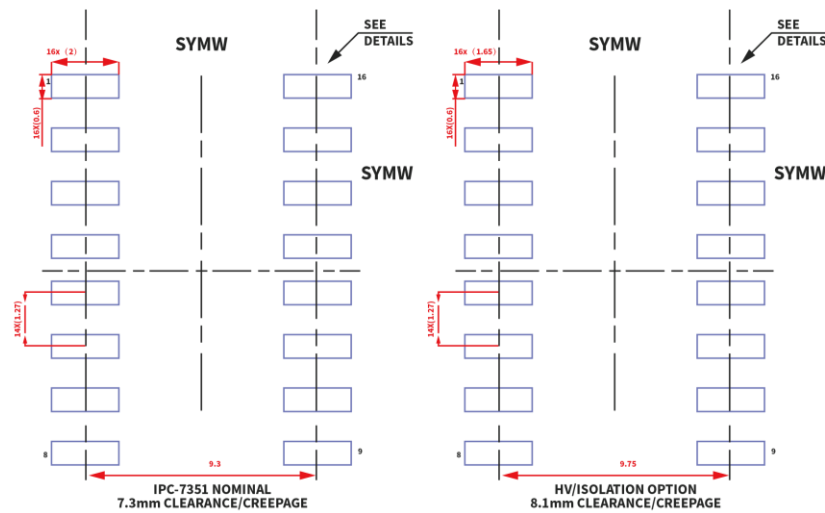


Figure 9.1 SOW16 Package Shape and Dimension in millimeters

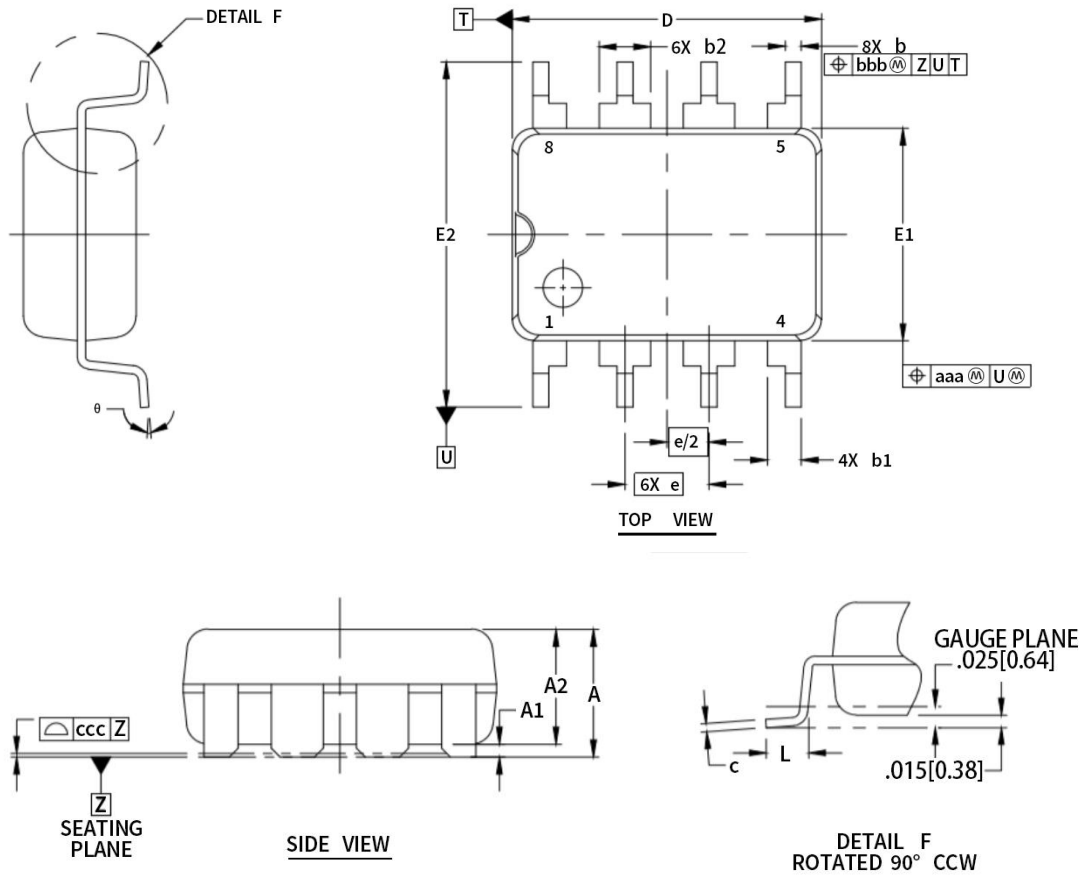


LAND PATTERN EXAMPLE(mm)



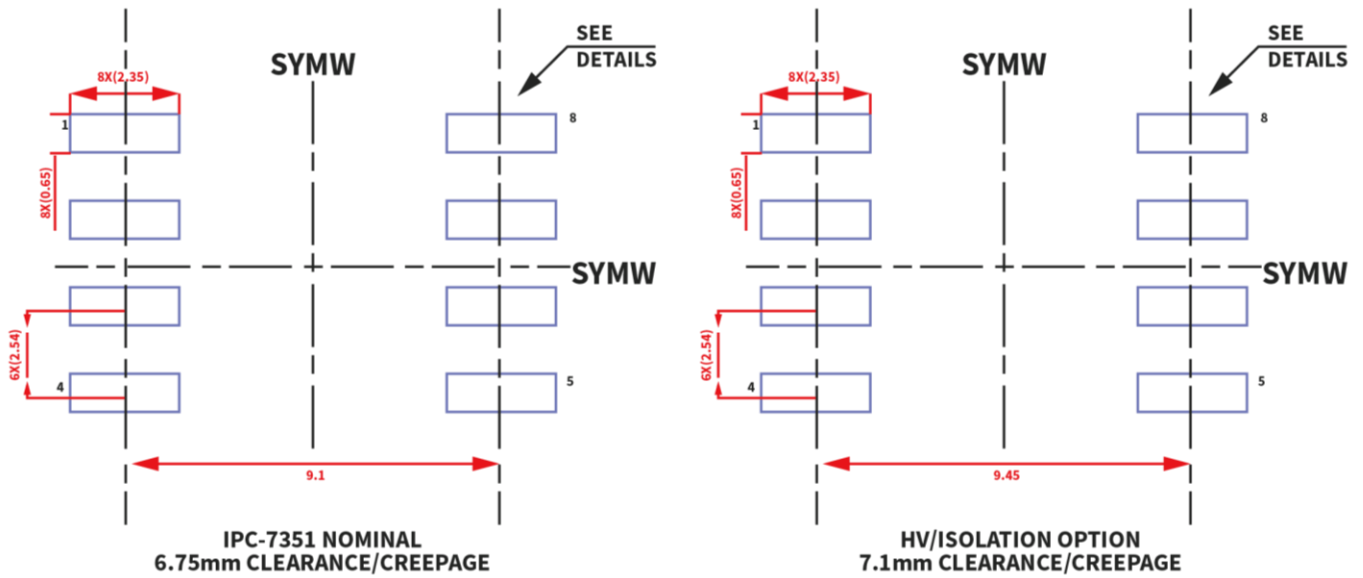
SOLDER MASK DETAILS

Figure 9.2 SOW16 Package Board Layout Example



|                 | SYMBOL | MIN     | NOM       | MAX   | MIN      | NOM       | MAX   |
|-----------------|--------|---------|-----------|-------|----------|-----------|-------|
| TOTAL THICKNESS | A      | .141    | ---       | .165  | 3.58     | ---       | 4.19  |
| STAND OFF       | A1     | .015    | ---       | .023  | 0.38     | ---       | 0.58  |
| MOLD THICKNESS  | A2     | .126    | ---       | .142  | 3.20     | ---       | 3.61  |
| LEAD WIDTH      | b      | .014    | ---       | .022  | 0.36     | ---       | 0.56  |
|                 | b1     | ---     | 0.039 REF | ---   | ---      | 0.99 REF  | ---   |
|                 | b2     | ---     | 0.06 REF  | ---   | ---      | 1.524 REF | ---   |
| L/F THICKNESS   | c      | .008    | ---       | .014  | 0.20     | ---       | 0.36  |
| BODY SIZE       | D      | .365    | ---       | .369  | 9.27     | ---       | 9.37  |
|                 | E1     | .244    | ---       | .260  | 6.20     | ---       | 6.60  |
|                 | E2     | .398    | ---       | .421  | 10.11    | ---       | 10.69 |
| LEAD PITCH      | e      | 100 BSC |           |       | 2.54 BSC |           |       |
| LEAD LENGTH     | L      | .0453   | ---       | .0571 | 1.15     | ---       | 1.45  |
|                 | θ      | 0°      | ---       | 8°    | 0°       | ---       | 8°    |
| LEAD OFFSET     | aaa    | .010    |           |       | 0.254    |           |       |
|                 |        |         |           |       |          |           |       |
|                 |        |         |           |       |          |           |       |
|                 |        |         |           |       |          |           |       |
|                 |        |         |           |       |          |           |       |

Figure 9.3 DUB8 Package Shape and Dimension in millimeters



**LAND PATTERN EXAMPLE(mm)**



**SOLDER MASK DETAILS**

Figure 9.4 DUB8 Package Board Layout Example

**10. Order information**

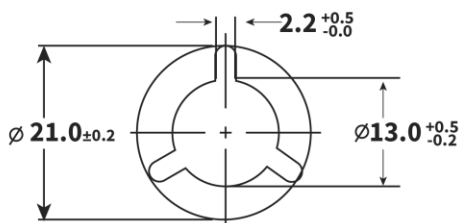
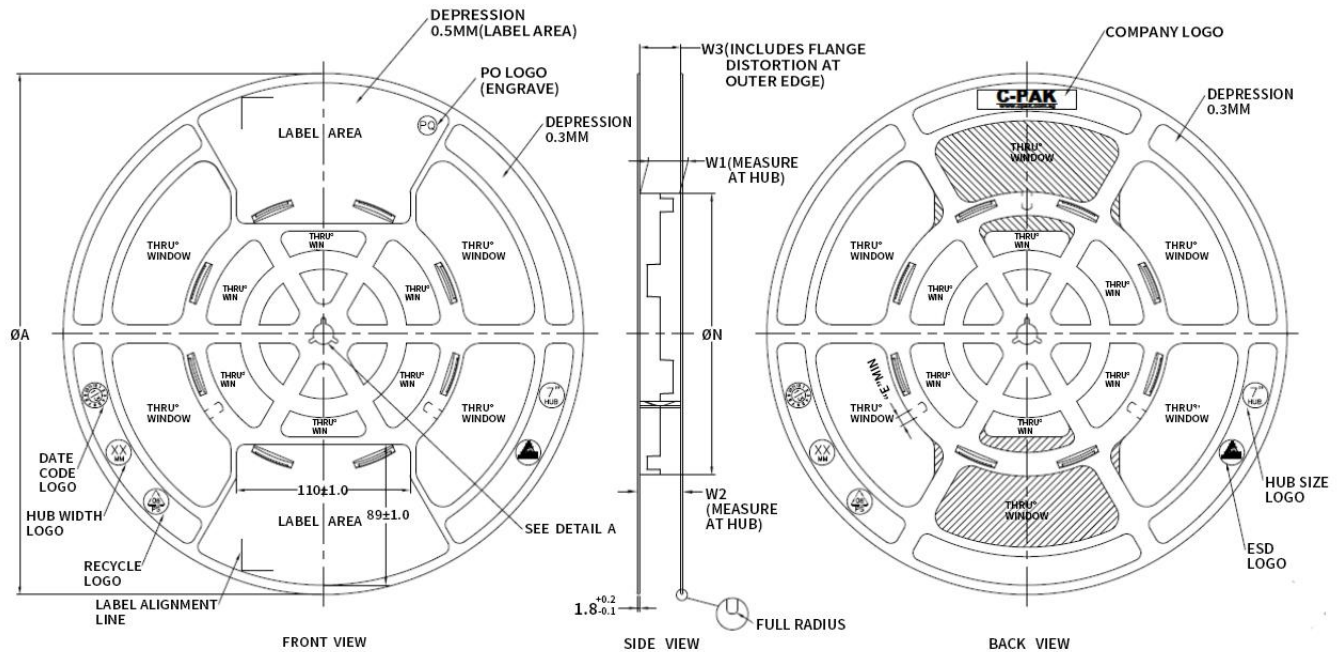
| <i>Part Number</i> | <i>Isolation Rating (kV)</i> | <i>Max Data Rate (Mbps)</i> | <i>Temperature</i> | <i>MSL</i> | <i>Package Type</i> | <i>Package Drawing</i> | <i>SPQ</i> |
|--------------------|------------------------------|-----------------------------|--------------------|------------|---------------------|------------------------|------------|
| NSi1050-DDBR       | 3                            | 1                           | -40 to 125°C       | 3          | DUB8                | DUB8                   | 800        |
| NSi1050-DSWR       | 5                            | 1                           | -40 to 125°C       | 2          | SOW16 (300mil)      | SOW16                  | 1000       |

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

**11. Documentation Support**

| <i>Part Number</i> | <i>Product Folder</i>      | <i>Datasheet</i>           | <i>Technical Documents</i> | <i>Isolator selection guide</i> |
|--------------------|----------------------------|----------------------------|----------------------------|---------------------------------|
| NSi1050            | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a>      |
|                    |                            |                            |                            |                                 |
|                    |                            |                            |                            |                                 |

## 12. Tape and Reel Information

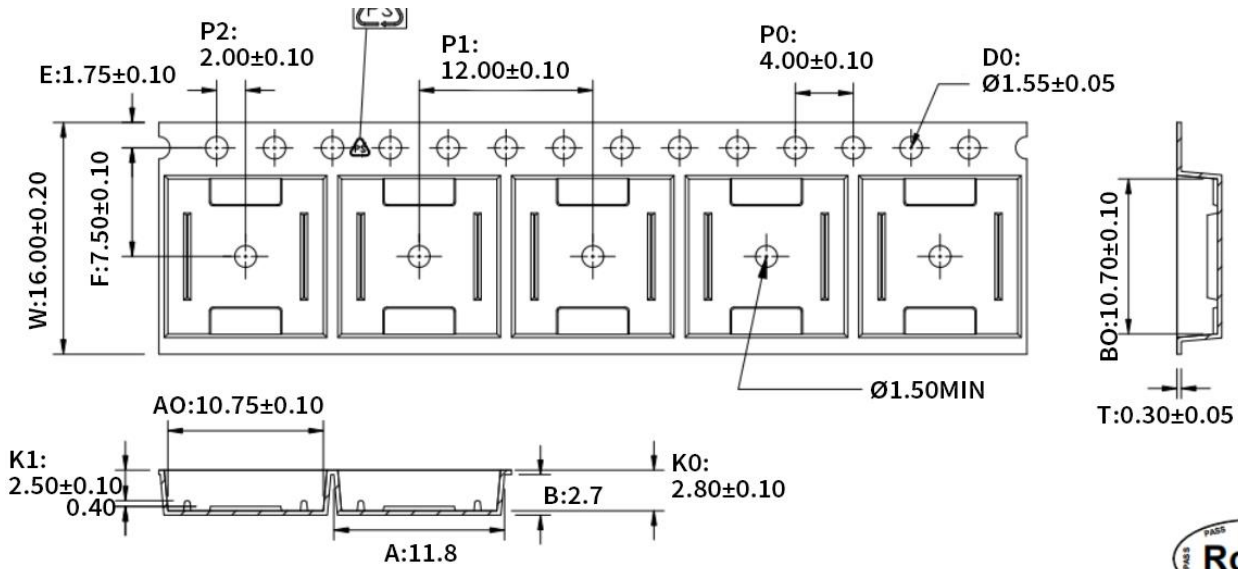


### PRODUCT SPECIFICATION

| TAPE WIDTH | $\varnothing A$<br>$\pm 2.0$ | $\varnothing N$<br>$\pm 2.0$ | W1                                   | W2<br>(Max) | W3  | E<br>(MIN) |
|------------|------------------------------|------------------------------|--------------------------------------|-------------|---|------------|
| 08MM       | 330                          | 178                          | 8.4 <sup>+1.5</sup> <sub>-0.0</sub>  | 14.4        | SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE | 5.5        |
| 12MM       | 330                          | 178                          | 12.4 <sup>+2.0</sup> <sub>-0.0</sub> | 18.4        |   | 5.5        |
| 16MM       | 330                          | 178                          | 16.4 <sup>+2.0</sup> <sub>-0.0</sub> | 22.4        |   | 5.5        |
| 24MM       | 330                          | 178                          | 24.4 <sup>+2.0</sup> <sub>-0.0</sub> | 30.4        |   | 5.5        |
| 32MM       | 330                          | 178                          | 32.4 <sup>+2.0</sup> <sub>-0.0</sub> | 38.4        |   | 5.5        |

### SURFACE RESISTIVITY

| LEGEND | SR RANGE              | TYPE                 | COLOUR     |
|--------|-----------------------|----------------------|------------|
| A      | BELOW $10^{12}$       | ANTISTATIC           | ALL TYPES  |
| B      | $10^6$ TO $10^{11}$   | STATIC DISSIPATIVE   | BLACK ONLY |
| C      | $10^5$ & BELOW $10^5$ | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E      | $10^9$ TO $10^{11}$   | ANTISTATIC (COATED)  | ALL TYPES  |



|    |            |
|----|------------|
| W  | 16.00±0.20 |
| A0 | 10.75±0.10 |
| B0 | 10.70±0.10 |
| K0 | 2.80±0.10  |
| K1 | 2.50±0.10  |

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$  mm.
6. Packing length per 22" reel: 378 Meters. (復卷 N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

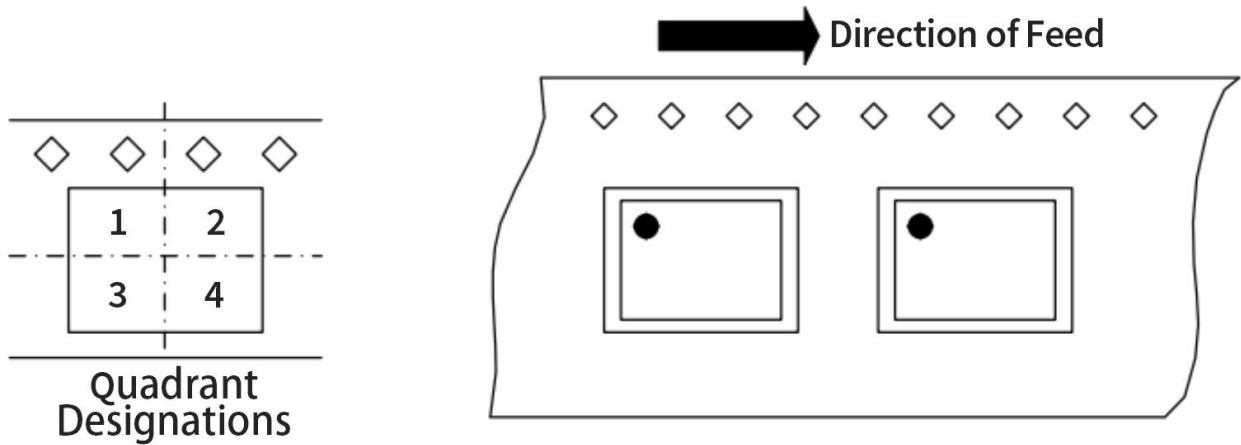
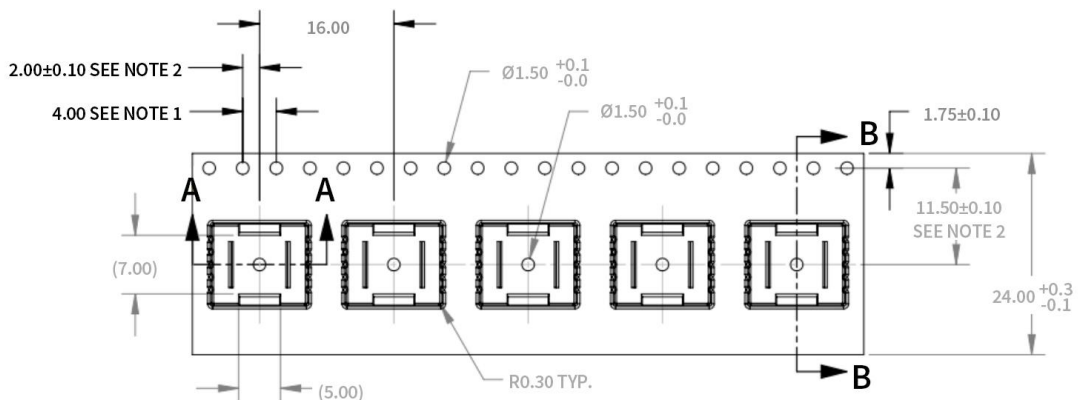


Figure 12.1 Tape and Reel Information of SOW16



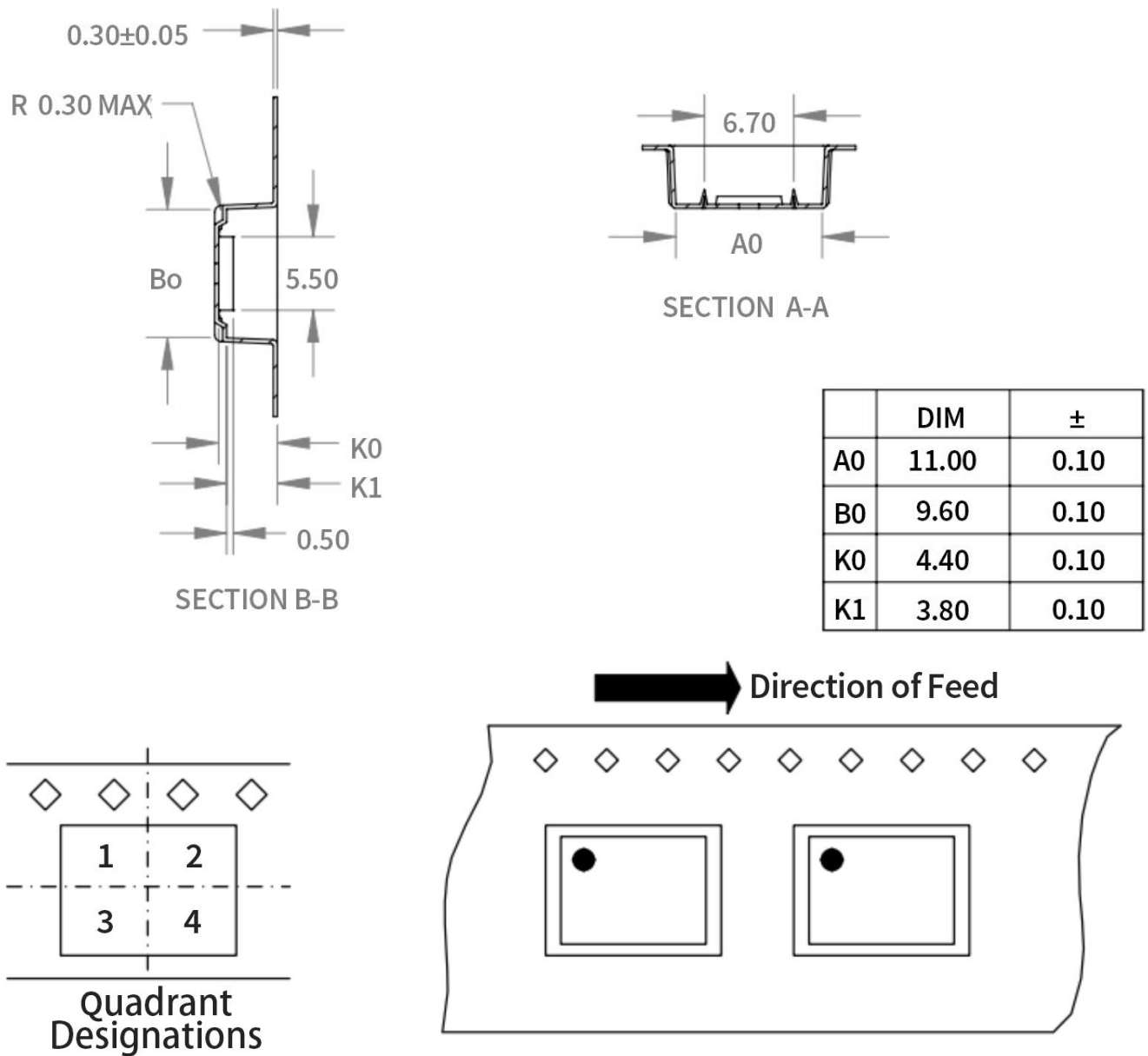


Figure 12.2 Tape and Reel Information of DUB8

### 13. Revision History

| Revision | Description  | Date       |
|----------|--|------------|
| 1.0      | Initial version  | 2020/8/7   |
| 1.1      | Changed tape and reel information  | 2020/12/20 |
| 1.2      | Added DUB8 tape and reel information   | 2021/3/1   |
| 1.3      | Update Regulatory information  | 2021/4/13  |
| 1.4      | Added reel direction of feed, corrected driver and receiver delay and UL Isolation voltage | 2022/6/7   |
| 1.5      | Update DUB8 Package Board Layout Example   | 2022/8/26  |



## **IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense ([www.novosns.com](http://www.novosns.com)).

**Suzhou Novosense Microelectronics Co., Ltd**