Application Note

NOVOSENSE

NSD1624-DSPKR Demo Board User Guide

AN-15-0008

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NSD1624-DSPKR
Demo Board User Guide

FEATURES

The NSD1624 demo board is designed to test NSD1624-DSPKR electronic characteristic. The related pins have been drawn out to the test pad TP3, TP5, TP7 and TP9. User can test the performance according to the request.

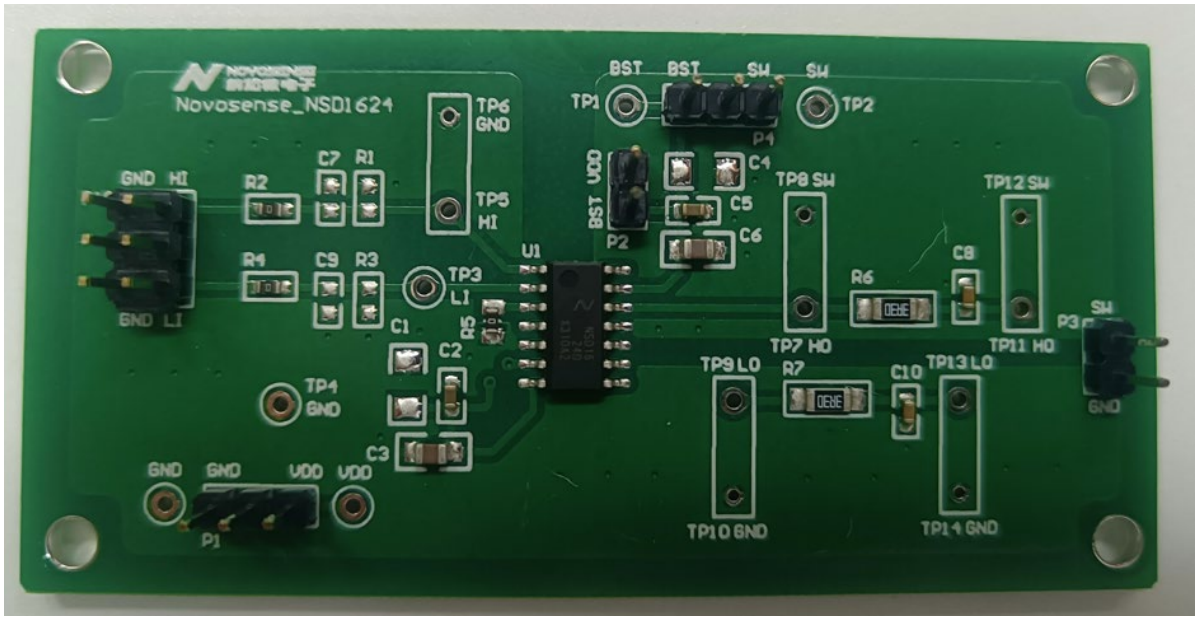

Figure 1. NSD1624 Demo Board

AN-15-0008

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INDEX

1.Demo Board Overview

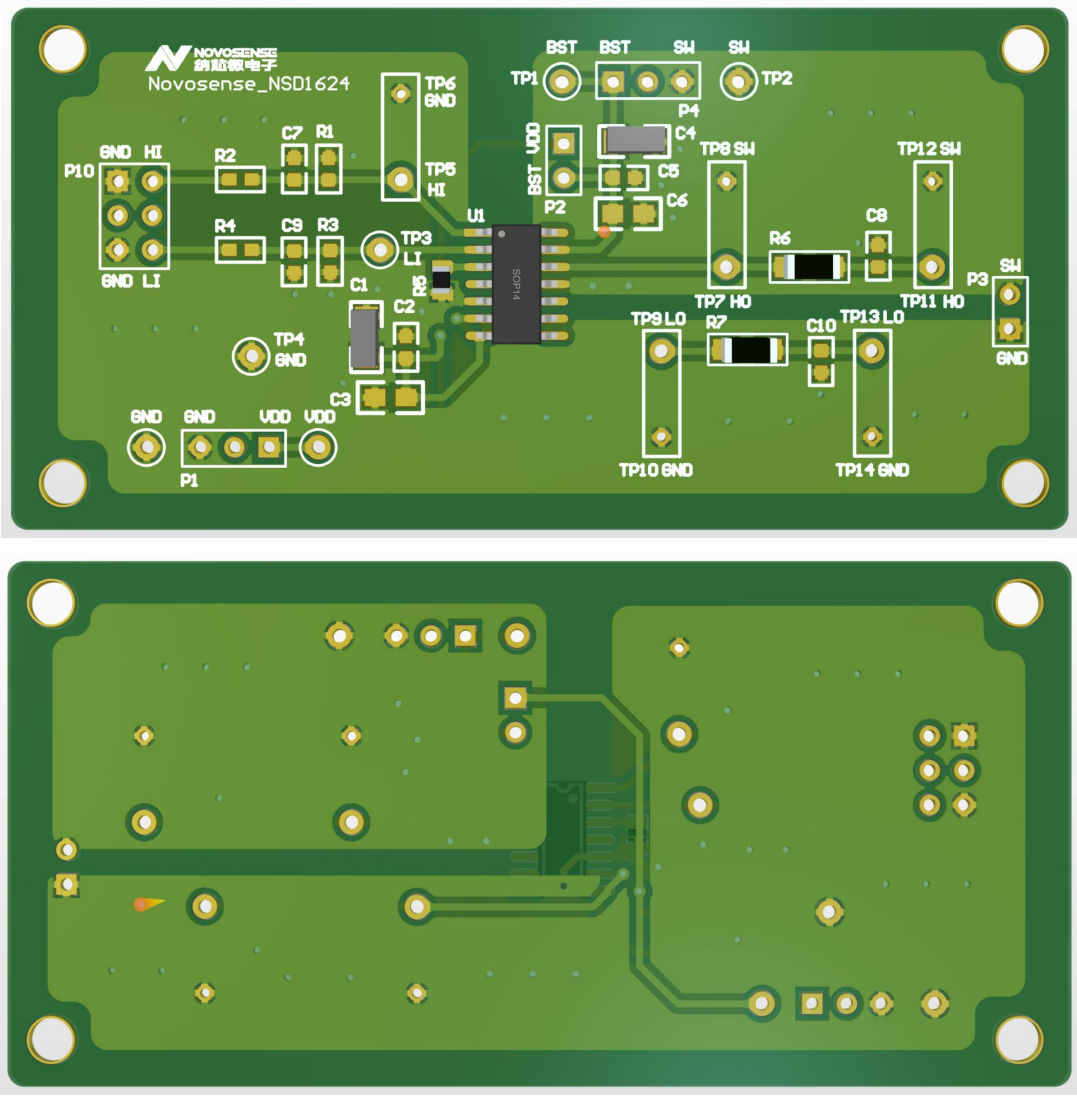

Figure 2. NSD1624-DSPKR Demo Board 3D (Bottom is flipped)

Board size： 78.2mm x 38.6mm x 1.6mm
Board Layers: 2 Layers
Connector pitch： 2.54mm

Table 1. Pin Configuration and Description

Connector	Description
P1	Voltage input VDD and GND.
P2	Jumper cap between VDD and BST
P3	Jumper cap between GND and SW
P4	High-side power supply BST and return reference SW.
P10	input HI and input LI.

Table 2. BOM list

Designator	Description	Value	Manufacturer	Part Number
C2, C5	0603, Capacitors, ceramic, X7R, general purpose	100nF	Murata	GRM188R72A104KA35#
C3, C6	0805, Capacitors, ceramic, X7R, general purpose	2.2uF	Murata	GCM21BR71E225KA73#
C8, C10	0603, Capacitors, ceramic, X7R, general purpose	1nF	Murata	GCD188R71H102KA01#
R2, R4, R5	0603, Resistors	0Ω	UNI-ROYAL	0603WAF0000T5E
R6, R7	1206, Resistors	3.3Ω	UNI-ROYAL	1206W4F033JT5E
U1	NSD1624-DSPKR	NSD1624-DSPKR	Novosense	/
P1,P4	2.54mm pitch 1X 3 , Connector			
P2,P3	2.54mm pitch 1X 2, Connector			
P10	2.54mm pitch 2X3, Connector			

2.Demo Board Introduction

The demo board can normally operate when it is powered by 10~20V DC power on VDD and BST. P2 is the jump cap between BST and VDD; P3 is the jump cap between SW and GND. The power supply between BST and SW can be independently provided or use the same power supply between VDD and GND according to user's require.

The terminal strip P5 is used for high-side and low-side PWM input. Two 0Ω resistors have welded at R2 and R4 to connect input to HI and LI pins, while the locations of R1, R3, C7 and C9 have been reserved to debug. R6 and C8 are used as HO output load and R7 and C10 are used as LO output load. HI, LI, HO and LO have been drawn to the test points that can observe the corresponding signal waveforms of NSD1624.

3.Application Notes

The demo board is 2 layers with 1oz copper and the minimum distance between SW and GND is only 70mil on board. The demo board is intended for function test use only and high voltage applications should be noted.

It is recommended that users avoid shaping the input signals to the gate driver in attempt to slow down the signal at the output. However, a small input filter can be used to filter out the ringing introduced by test interference. Users can change the resistors and capacitors at R2, R4, C7 and C9. It should be noted that changing these parameters would affect the propagation delay time and other parameters.

The load capacitance is 1nF and the load resistor is selected 3.3 Ω. It is normal for ring caused by the parasitic inductance as shown in Figure 3. The resistance value can be increased to solve this problem.

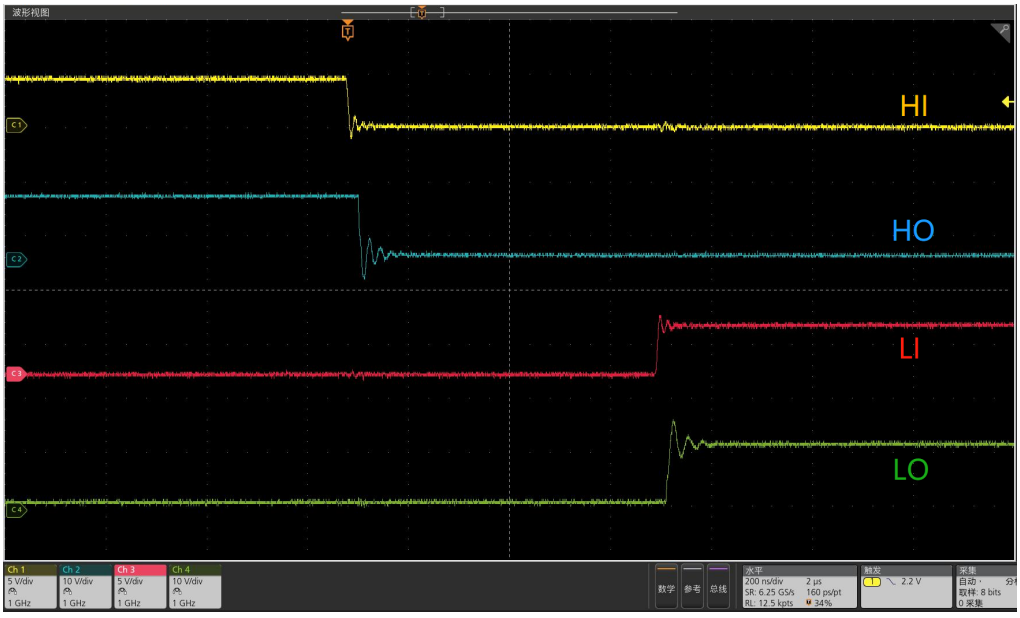

Figure 3. Input and output waveforms

4.Schematic and PCB Layout of Demo Board

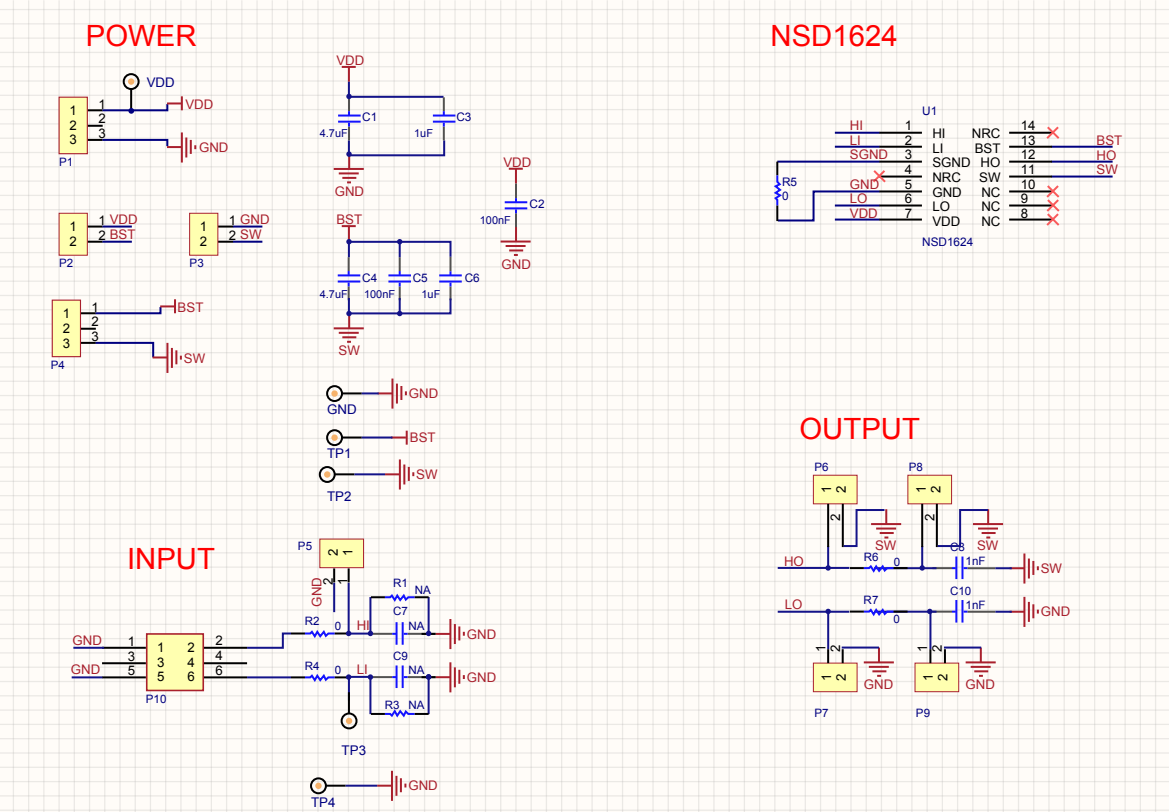

Figure 4. Schematic

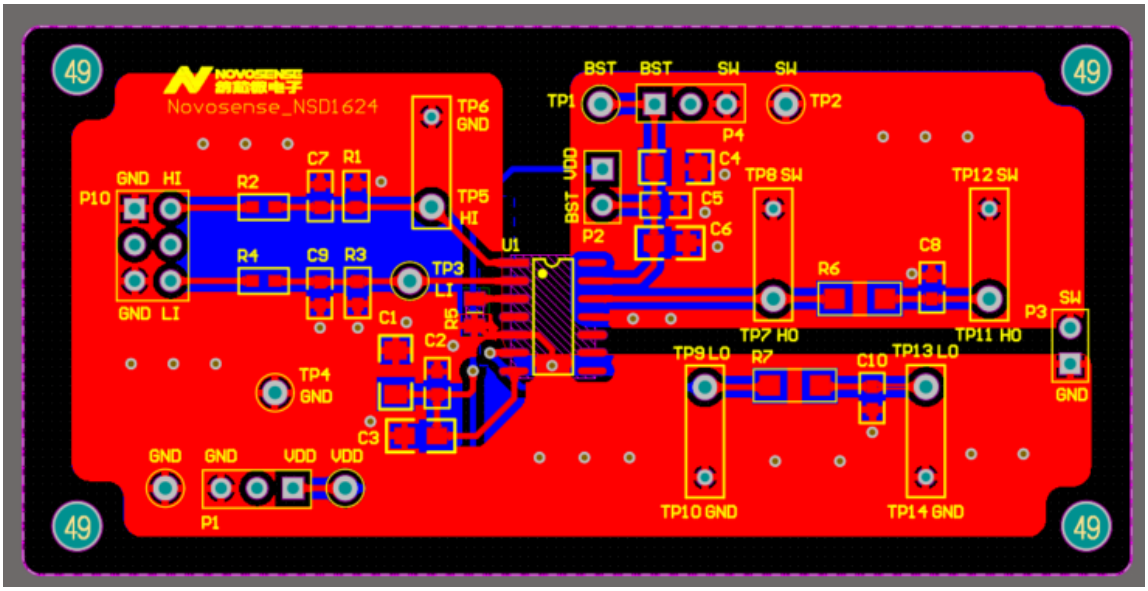

Figure 5. Top Layer

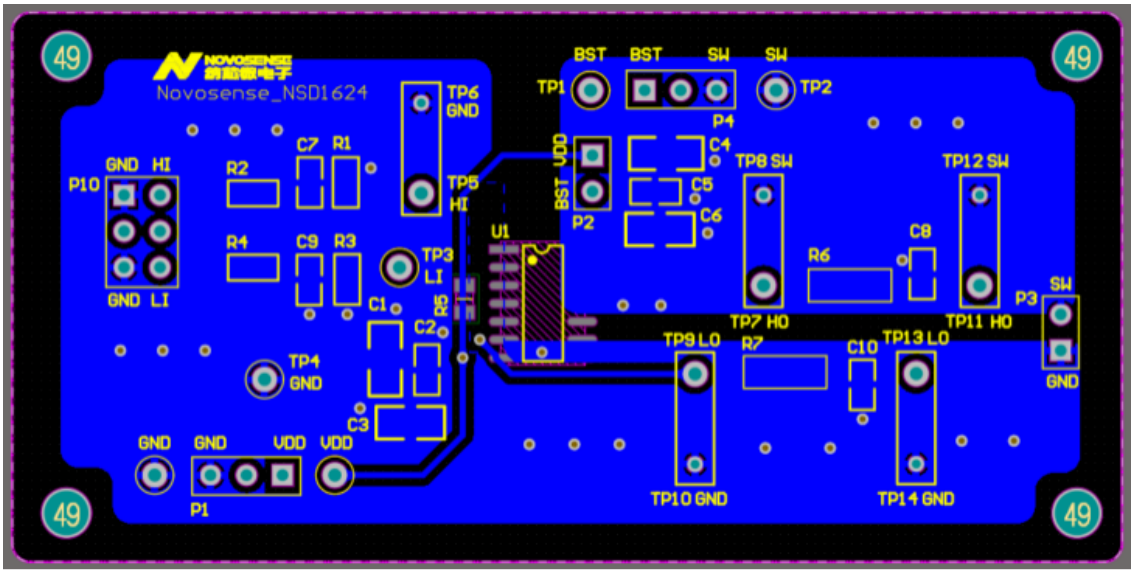

Figure 6. Bottom Layer

5.Revision History

Revision	Description	Author	Date
1.0	Initial version	Long Huojun	2/11/2023

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