NSD5604E / NSD5604NE

4-channel Low Side Driver

Datasheet (EN) 1.1

Product Overview

The NSD5604E / NSD5604NE is a 4-channel low side driver for industrial applications including programmable logic control, general relays, or other solenoid drivers.

The device includes 4x parallel input interface, which controls 4x independent driving outputs for resistive, inductive, or capacitive loads. The output channels can be parallelized to support high current load and reduce device power dissipation. Low side outputs are protected against over temperature and short circuit through embedded temperature sensor, adjustable load current limitation and cut off timing functions setting by ILIM and COD pins external connection.

The integrated diodes clamp the voltage transients generated during inductive loads turning off; combined with different external TVS connection topologies, slow decay or fast decay turn-off can be implemented.

NSD5604E also features an additional 5V max 20mA LDO output for on board digital isolator or photo coupler power supply.

Both NSD5604E & NSD5604NE are available in a compact 20-pin, 6.5mm x 6.4mm HTSSOP20 package, specified over -40 to 125°C operating temperature range.

Applications

- PLCs
- General relays
- Solenoid drivers
- Unipolar stepper motor drivers

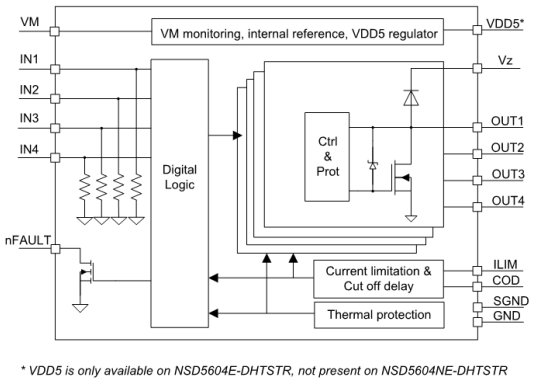
Device Information

Part Number	*Package*	*Body Size*
NSD5604E-DHTSTR	HTSSOP20	6.5mm X 6.4mm
NSD5604NE-DHTSTR	HTSSOP20	6.5mm X 6.4mm

Key Features

- 4x low side driver
  - Individual PWM input control interface, up to 200kHz
  - Low side driver output can be parallel
  - High speed trise and tfall
- Typical operating load current: 0.5 A (per channel) / 2 A (one channel)
- Integrated active clamping or integrated catch diodes for external Vz (clamp) path in inductive load fast switch off
- Load current limitation adjust by external resistor
- Short circuit protection cut off timing delay adjust by external resistor
- Wide operating ranges from 8v to 50v
- Integrated LDO regulator 5v / 20mA output (NSD5604E version only)
- Integrated protection
  - Overcurrent / short circuit protection
  - Both common thermal and per channel over temperature protection
  - VM input undervoltage protection
  - Dedicated nFault indicator pin
- RoHS& REACH Compliance
- HTSSOP20, 6.5mm X 6.4mm with exposed PAD

Functional Block Diagrams



** VDD5 is only available on NSD5604E-DHTSTR, not present on NSD5604NE-DHTSTR*

Figure 0.1 NSD5604E/ NSD5604NE Block Diagram

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1. Pin Configuration and Functions

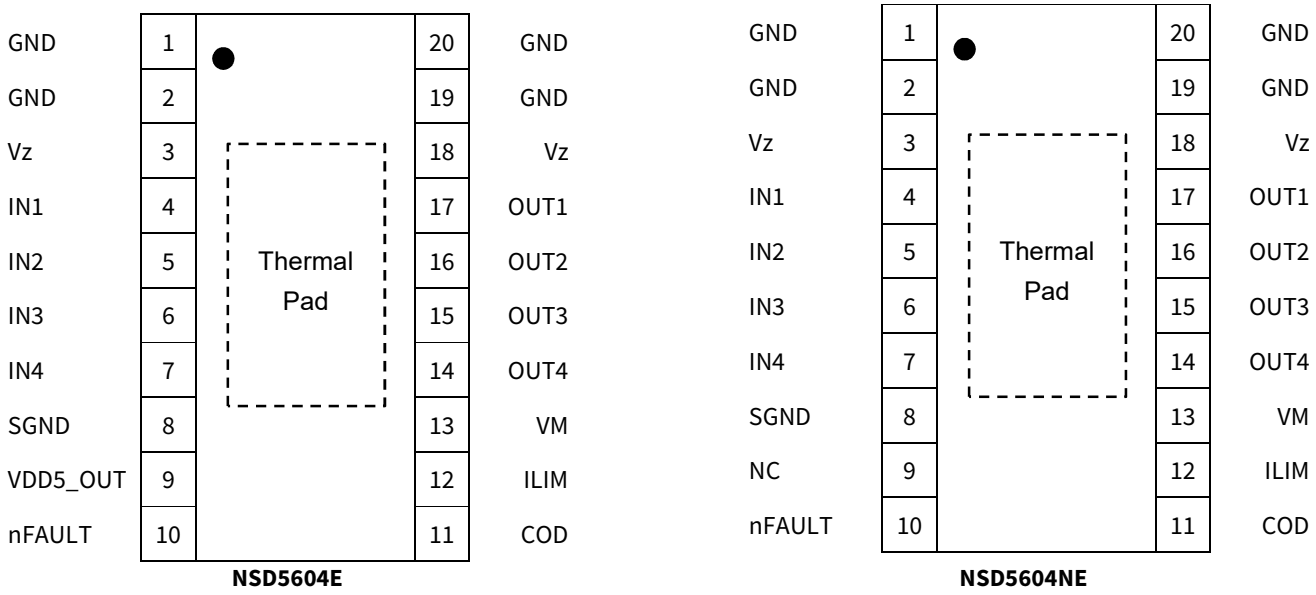


Figure 1.1 NSD5604E and NSD5604NE Pinout

Table 1.1 NSD5604E and NSD5604NE Pin Configuration and Description

SYMBOL	NSD5604NE PIN NO.	NSD5604E PIN NO.	TYPE	DESCRIPTION
GND	1, 2, 19,20		Power Supply	Integrated power switch ground
Vz	3, 18		Output	Load clamp voltage pins. Pins 3 and 18 must be shorted on the application board and then connected directly to the supply rail, or by an external Zener or TVS diode to the supply rail or to PGND
IN1	4		Input	Channel 1 input, drive high to turn on low side OUT1
IN2	5		Input	Channel 2 input, drive high to turn on low side OUT2
IN3	6		Input	Channel 3 input, drive high to turn on low side OUT3
IN4	7		Input	Channel 4 input, drive high to turn on low side OUT4
SGND	8		Power Supply	Logic interface block ground
VDD5	-	9	Output	VDD5 output pin, recommend 47nF X7R ceramic capacitor close to VDD5 pin
NC	9	-	NC	Not connected
nFAULT	10		Output	Fault output pin, open drain, logic low when in fault condition.

COD	11	Input	Programmable cut-off delay during overcurrent operation. It cannot be left floating: connect to PCB SGND ground plane to disable the cut-off function or connect a resistor between COD and PCB ground to set the delay
ILIM	12	Input	Limitation current adjustment. It cannot be left floating: connect a resistor between ILIM and PCB ground to set the current limit threshold
VM	13	Power Supply	Supply voltage input, suggest >1uF capacitor.
OUT4	14	Output	Power stage, channel 4 output
OUT3	15	Output	Power stage, channel 3 output
OUT2	16	Output	Power stage, channel 2 output
OUT1	17	Output	Power stage, channel 1 output
Thermal PAD	-		Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VM	Power supply voltage	–0.3	55	V
Vz	Vz voltage	–0.3	VDEMAG	V
V_{INX}, V_{nFAULT}	Logic input/output voltage (INx, nFault)	–0.3	6	V
V_{OUTX}	Output voltage	–0.3	VDEMAG	V
VDD5_OUT	VDD5 pin voltage	–0.3	6	V
V_{ILIM}, V_{COD}	COD, ILIM pin voltage	–0.3	6	V

3. ESD Ratings

SYMBOL	PARAMETER	VALUE	UNIT
VESD	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±3000	V
	Charged device model (CDM), per JEDEC specification JS-002	±1000	V

4. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VM	VM Power supply voltage	8		50	V
Vz	Vz external clamp voltage	0		55	V
V_{INx}	Logic input voltage	0		5	V
f_{PWM}	Logic input PWM frequency (INx)	0		200	kHz

5. Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	Thermal resistance, junction to case		3		°C/W
Rthja	Thermal resistance, junction to ambient, on 2-layer PCB		50		°C/W
	Thermal resistance, junction to ambient, on 4-layer PCB		39		°C/W

6. Electrical Characteristics

Tj = 25°C, VM = 8 to 50V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		8		50	V
I_{VM}	VM operating supply current	VM = 24V, VDD5 no load			3	mA
V_{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers	6.5		7.5	V
		VM rises until operation recovers	7		8	V
V_{UVLO_HYS}	VM undervoltage hysteresis			500		mV
t_{UVLO}	VM undervoltage deglitch time			10		µs
Regulator (VDD5_OUT on NSD5604E)						
VDD5	VDD5 output voltage	0 to 20mA load current	4.65	5	5.35	V
I_{VDD5_LIMIT}	VDD5 load current limitation	VDD5 short to GND	20		35	mA
V_{line_VDD5}	VDD5 line regulation	VM = 8V to 50V, Load current 20mA, Cvdd5 = 47nF			30	mV
V_{load_VDD5}	VDD5 load regulation	VM=24V, load current from 0mA to 20mA, Cvdd5 = 47nF			65	mV
V_{OS_VDD5}	VDD5 overshoot during power up				5.5	V
PSRR_VDD5	power supply ripple rejection	Design information f = 100kHz	40			dB
Logic Control Input (DIS, Reset, IN1, IN2, IN3, IN4)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic low current	VIN = 0 V	-5		5	µA
I_{IH}	Input logic high current	VIN = 5 V		50	100	µA
R_{PD}	Pulldown resistance	to GND		100		kΩ
Power stage output (OUT1 / OUT2 / OUT3 /OUT4)						
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 0.5 A, Ta=25		0.26	0.36	Ω
		VM = 24 V, I = 0.5 A, Ta=125			0.56	Ω

I_{LEAK_OUTx}	OFF-state leakage	VOUT = 24V	-10		10	μA
V_{DEMAG}	internal clamping voltage		53	58	65	V
t_{RISE}	Output rise time	VM = 24 V, OUTx rising from 10% to 90%, Resistive load		0.2		μs
t_{FALL}	Output fall time	VM = 24V, OUTx failing from 90% to 10%, Resistive load		0.2		μs
t_{PD}	Propagation delay	INx to OUTx OFF->ON		0.5	0.8	μs
		INx to OUTx ON->OFF		0.5	0.8	μs
Power stage output (Vz)						
V_{FCD}	Catch diode forward voltage	VM = 24 V, I = 0.5 A		1	1.2	V
I_{RCD}	Catch diode reverse current	Vrrm = 55 V			10	μA
Current limitation						
I_{LIM}	Current limitation threshold	0≤RLIM<20kΩ	3 +/- 30%			A
		30kΩ≤RLIM≤120kΩ	60/RLIM(kΩ) +/- 30%			A
t_{COD}	Cut off delay timing	0≤RCOD<20kΩ	Disable			
		60kΩ≤RCOD≤240kΩ	RCOD(kΩ)/120 +/-30%			ms
t_{RETRY}	Retry timing	60kΩ≤RCOD≤240kΩ	32*tCOD			
Thermal protection						
$T_{SD\_Central}$	Chip central thermal shutdown temperature		150	160	180	°C
$T_{SD\_Channel}$	thermal shutdown temperature		150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
nFault output						
V_{OL}	Output low voltage	Io = 2mA			0.5	V
I_{LEAK_nFAULT}	Output high leakage current	Vo = 5V			1	μA

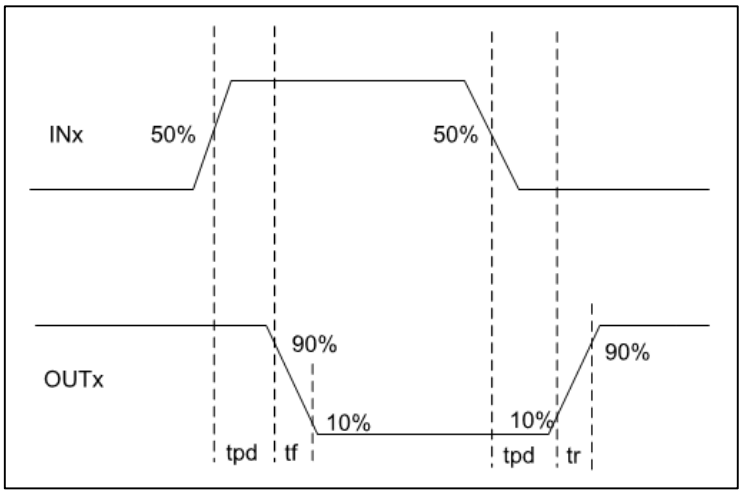


Figure 6.1 INx to OUTx propagation timing, OUTx rise timing and falling timing

7. Functional Description

7.1. VM & VM UV / OV protection

VM is the supply voltage, range from 8V to 50V with typical case 24V industrial power supply.

It is recommended to put at 1µF ceramic capacitor closed to VM pin.

When VM power supply pin voltage falls below the undervoltage threshold (V_{UVLO}) over 10µs typ. undervoltage deglitch time, low side outputs OUTx becomes OFF and internal logic are disabled. When VM rise above the V_{UVLO}, the device automatically resumes operation according to INx pin control table.

7.2. VDD5_OUT on NSD5604E

VDD5_OUT pin provides stable 5V linear regulator output to external load, such as digital isolator etc. Max 20mA load current capability is supported.

Load current limitation is integrated to against overcurrent or load short to ground fault condition.

It is recommended to put 47 or 100nF X7R ceramic type capacitor on VDD5_OUT for gain regulation loop stability.

It should be noted that internal linear regulator has high power dissipation when VM in high and high load current is drawn. The power dissipation (VM-VDD5) x I_{VDD5} result the self-heating of device, for example:

VM=24V, VDD5 average load current = 15mA, P_{VDD5} = (24-5) x 0.015 = 0.135w

When NSD5604E triggers internal thermal shut down, the VDD5 regulator is automatically turn off and nFault pin asserted. Normal operation will be resumed when internal junction temperature drops below TSD-T_{HYS}, and release nFAULT pin.

Note:

VDD5_OUT is NOT allowed to work as power source which directly connecting to external load of board outside without protection.

7.3. GND, SGND and Exposed Pad

GND internally connect to the source of low side MOSFET, and it is used as power ground. SGND stands for the signal ground and provide the reference level for logic interface.

GND and SGND pins must be externally shorted on the application board.

The exposed pad at the package bottom allows better heat dissipation. It must be connected to PCB ground for best thermal performance.

7.4. IN1, IN2, IN3, IN4 Input control

INx pin accepts the ON/OFF (high/low) or PWM (max 200kHz) input signal. When it is driven high, internal logic switch on the corresponding low side output channel, vice versa, setting INx low switches off the corresponding OUTx.

Each INx input pin has typ 100kohm internal pull-down resistance.

7.5. Low side output stage, OUT1 / OUT2 / OUT3 / OUT4

The four low side drivers are designed to drive inductive/resistive/capacitive load which connects between power supply and OUTx pins.

The four power stages can be in parallel to support higher load current.

7.6. Vz pin

The device integrates internal catch diode between each OUTx and common Vz pin. It provides different decay option according to Vz pin application external connection.

7.7. Protection function

7.7.1. VM undervoltage protection

When VM power supply pin voltage falls below the undervoltage threshold (V_{UVLO}) over 10µs typ. undervoltage deglitch time, low side outputs OUTx becomes OFF and internal logic are disabled. When VM rise above the V_{UVLO}, the device automatically resumes operation according to INx pin control table.

7.7.2. Overcurrent protection / current limitation ILIM & cut off delay

Two pins, ILIM and COD, control the overcurrent reaction threshold and cut off delay timing by setting external resistor on ILIM and COD pins. The selection guide of R_{ILIM} and R_{COD} are shown as below table 2 and 3.

Table 7.1 ILIM and its function table

R_{ILIM} resistor between ILIM and GND	Function behavior
$0 \le R_{ILIM} < 20k\Omega$	I_{LIM} internally limited to 3A typ
$30k\Omega \le R_{ILIM} \le 120k\Omega$	I_{LIM} internally limited to 60/RLIM(kΩ) typ
$120k\Omega \le R_{ILIM}$	I_{LIM} internally limited to 60/RLIM(kΩ) typ, linearity is not guaranteed

Table 7.2 COD and its function table

R_{COD} resistor between COD and GND	Function behavior
$0 \le R_{COD} < 20k\Omega$	Cut off delay internally disabled, IC protected by thermal shutdown
$60k\Omega \le R_{COD} \le 240k\Omega$	t_{COD}, cut off delay, limited to RCOD(kΩ)/120 ms $t_{RETRY,}$ restart delay, 32 x t_{COD}

In case of I_{LIM} threshold is triggered, the corresponding low side output moves to current limitation condition ($I_{LOAD} = I_{LIM}$) at least for t_{COD}. If the load current limit persists for longer than the t_{COD} time, the low side output will be disabled and nFAULT pin driven low. The driver will remain disabled for t_{RETRY}, then the fault will be automatically cleared, and output retry to switch on if INx remains high state. See figure 4 for current limitation and cut off delay behavior.

If one of four channel triggers current limitation protection, other channels remain normal operation until fault condition like common over temperature happens.

Note:

During current limitation condition, low side output power dissipation is calculated as

$P_{OUTX\_ILIM} = V_{OUTX} \times I_{LIM} = (V_{LOAD} - I_{LIM} \times R_{LOAD}) \times I_{LIM}$

For example, RILIM = 80kohm, VLOAD = 24V, RLOAD = 1ohm

ILIM = 60/80 = 0.75A

$P_{OUTX\_ILIM} = V_{OUTX} \times I_{LIM} = (V_{LOAD} - I_{LIM} \times R_{LOAD}) \times I_{LIM} = (24 - 1 \times 0.75) \times 0.75 = 17.4w$

If $60k\Omega \le R_{COD} \le 240k\Omega$, $P_{OUTX\_ILIM\_AVERAGE} = P_{OUTX\_ILIM} X\ t_{COD} / t_{COD} + t_{RETRY} = P_{OUTX\_ILIM} / 33 = 17.4 / 33 = 0.53w$

If $R_{COD} = 0$, $P_{OUTX\_ILIM\_AVERAGE} = P_{OUTX\_ILIM} = 17.4w$, *device is protected by thermal shutdown.*

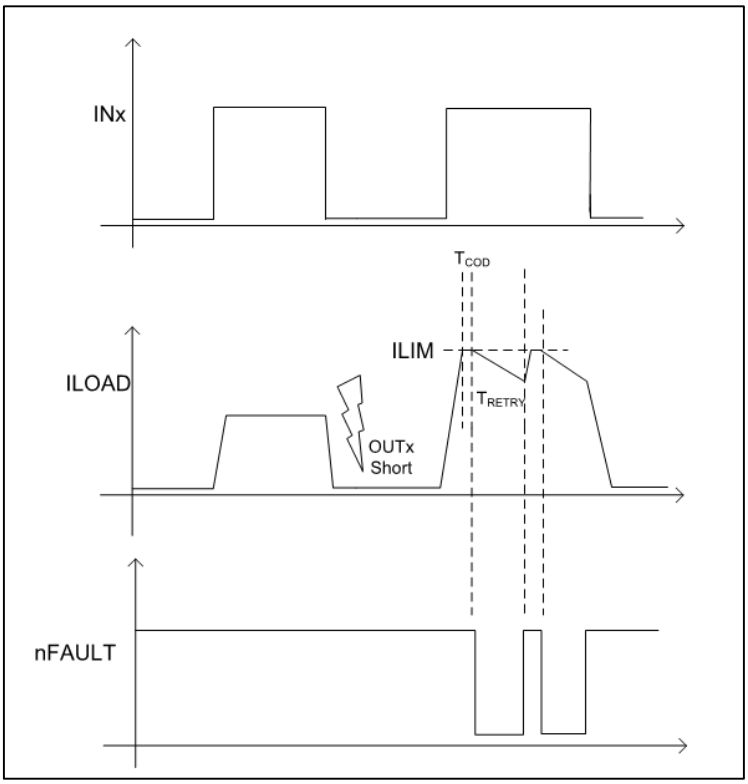


Figure 7.1 Current limitation ILIM & cut off delay behavior

7.7.3. Over temperature

To protect power stage from overheat, a dedicated thermal sensor is placed close to each power MOSFET, once the sensed temperature over TSD_Channel threshold, the corresponding power MOSFET channel is automatically disabled and nFAULT pin assert low.

The thermal protection of 4x output power stages is independent.

The device also monitors die central temperature. It will disable all four power MOS and VDD5 outputs when central temperature rises above TSD_Central.

Normal operation will be resumed when the temperature drops below TSD-T_{HYS}, and release nFAULT pin.

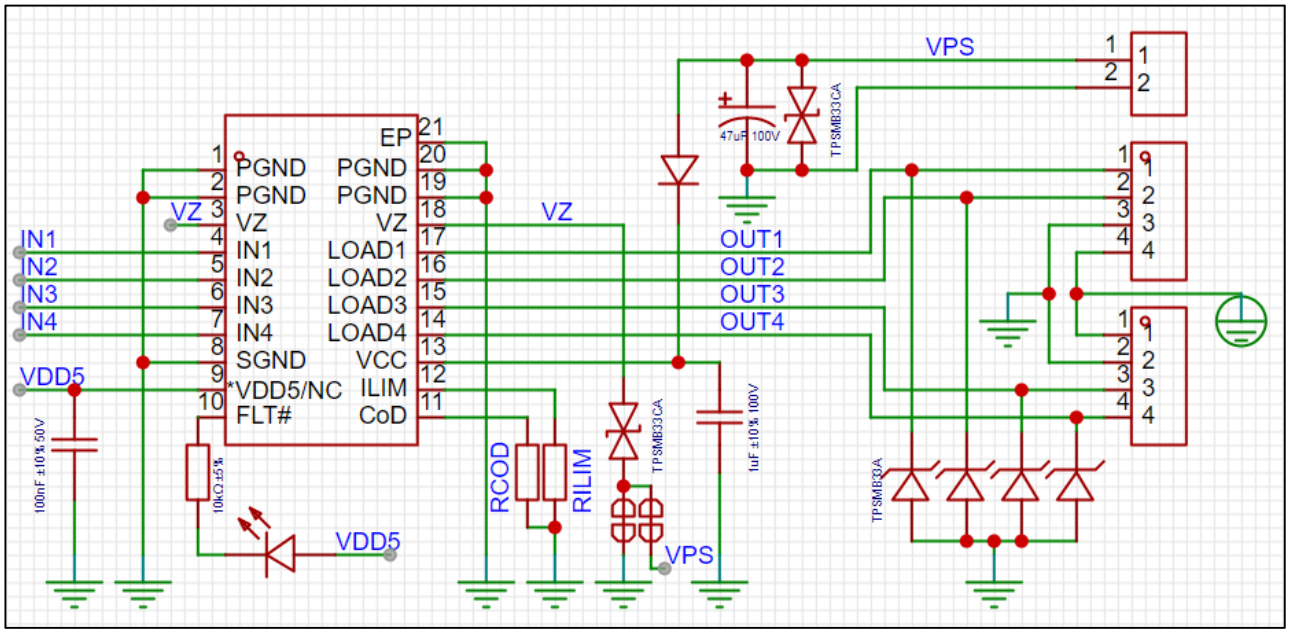
7.7.4. nFault Protection Summary

Table 7.3 nFAULT & low side behavior vs. Fault condition

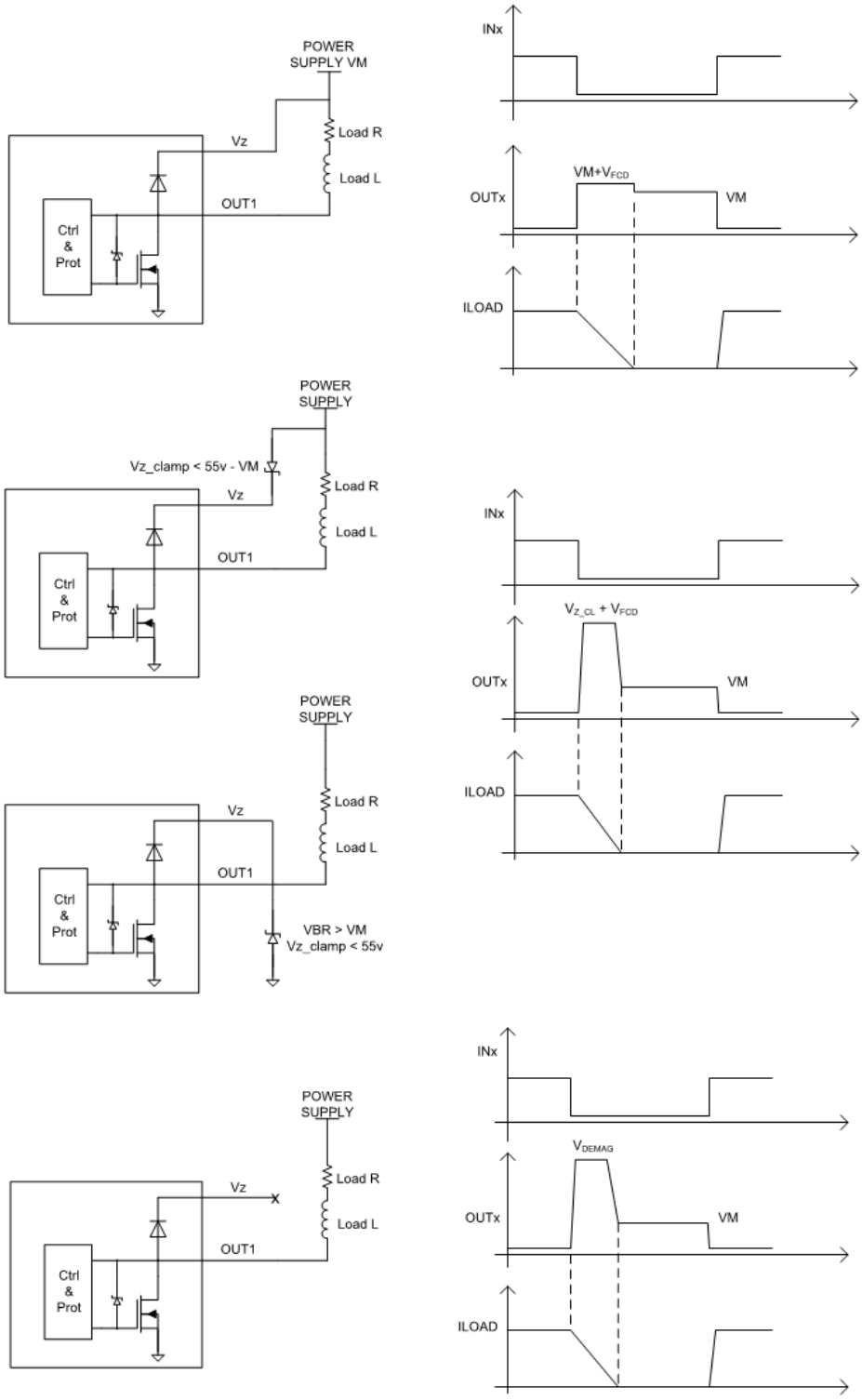
Fault	Condition	nFAULT status	Low side	Recovery procedure
VM undervoltage	VM < VUVLO	LOW	OFF	VM > VUVLO
OCP	I > ILIM	LOW	OFF	Auto retry depends on Cut off delay and INx
Over temperature	Low side T_J > TSD_channel or T_J> TSD_Central	LOW	OFF	TJ < TSD - THYS

8. Application information

8.1. Typical circuit in PLCs application

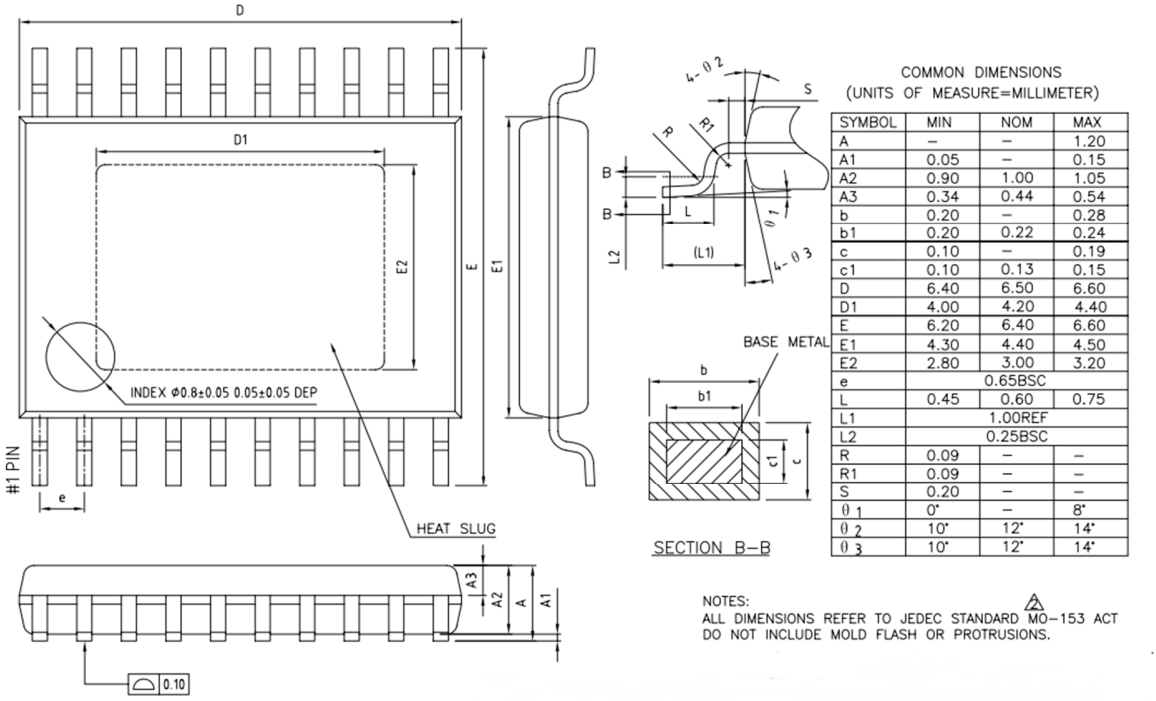


8.2. Slow decay and fast decay with external or internal active clamping



9. Package Information

9.1. HTSSOP20 package information

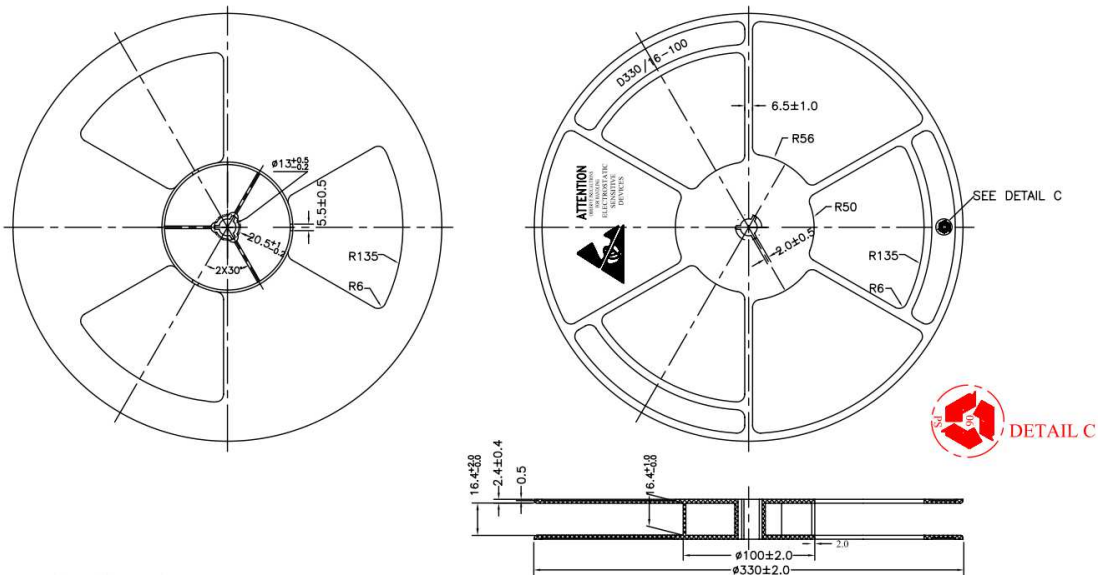


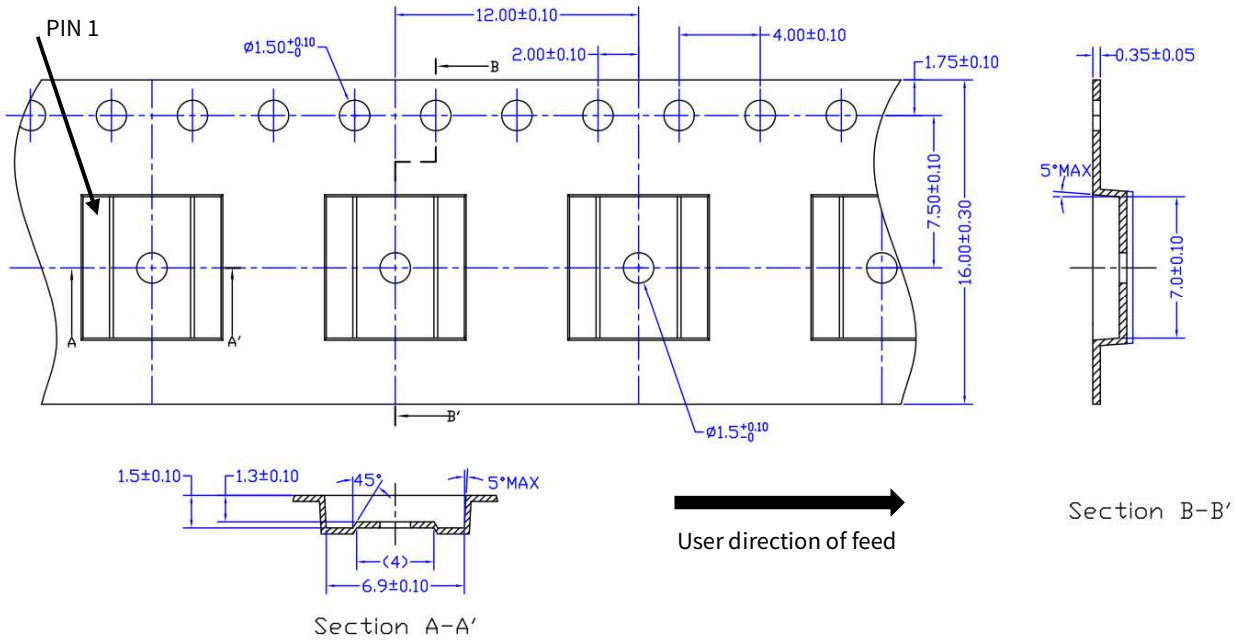
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
D1	4.00	4.20	4.40
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 ACT
2. DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

9.2. HTSSOP20 packaging information





10. Ordering Information

Part Number	Adjusted ILIM / Cut Off Delay	VDD5_OUT	Package Type	MSL	SPQ
NSD5604E-DHTSTR	YES	YES	HTSSOP20	3	3000
NSD5604NE-DHTSTR	YES	NO	HTSSOP20	3	3000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.					

11. Revision History

Revision	Description	Date
1.0	Initial version	2022/12/8
1.1	Template update	2023/10/17

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