NOVOSENSE

NSD1026V-Q1
High Speed, 5A Dual-Channel, Low-Side Gate Driver with Enable

Datasheet (EN) 1.0

Product Overview

NSD1026V is a wide supply, non-inverting, dual-channel, high speed, low side gate driver for both MOSFET, and IGBT. It has capability to deliver 5A sink and source current to the capacitive load along with rail-to-rail output to reduce the Miller effect during MOSFET's switching transition. Fast rise and fall times as well as matched propagation delay of both output channels enable the NSD1026V suitable for high frequency power converter application.

Both the input and enable pins of NSD1026V has ability to handle -10V which enhance the noise immunity and robustness of the device. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers.

The internal circuitry provides an under voltage lockout (UVLO) function by holding the output low until the supply voltage is under the UVLO threshold values. Wide band of VDD hysteresis between high and low thresholds offers excellent noise immunity. The NSD1026V automotive device is available in SOP8, HMSOP8, and HSOP8 package with operating junction temperature range from -40℃ to 125℃.

Key Features

- AEC-Q100 qualified
  - Temperature grade 1：-40℃ to 125℃
- Wide supply voltage range: 5V to 26V
- Source/Sink drive current: ±5A (Peak)
- Two independent enable pins to control channel output
- Ability to handle negative swing of (-10V) at each input pin
- CMOS/TTL compatible logic inputs
- 5A reverse current feature eliminates the need of output protection circuitry
- Operating temperature range: -40℃ to 125℃
- Low supply current
- Short propagation delays: 19ns (typical)
- RoHS-compliant package

Applications

- Typical SMPS (Solar, Server, Telecom, Industrial)
- Motor Controllers
- Pulse Transformer Driver
- DC-DC Converters
- Class-D switching amplifier
- Line-drivers

Device Information (1)

Part Number	Package	Body Size
NSD1026V-Q1SPR	SOP8	4.9 mm × 3.9 mm
NSD1026V-Q1HSPR	HSOP8	4.9 mm × 3.9 mm
NSD1026V-Q1HMSR	HMSOP8	3.0 mm × 3.0 mm

1) For all available packages, and order information refer to the end of datasheet.

Functional Block Diagrams

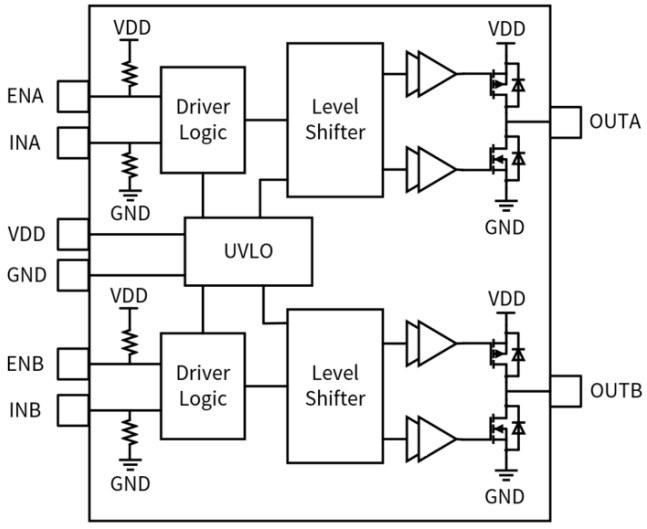

Figure 1. NSD1026V Block Diagram

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1. Pin Configuration and Functions

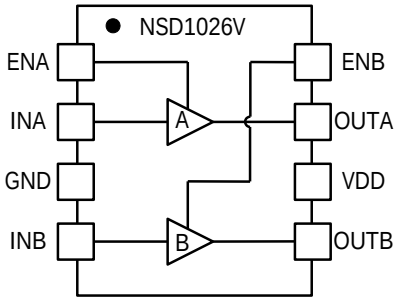


Figure 1.1 NSD1026V Package

Table 1.1 NSD1026V Pin Configuration and Description

NSD1026V PIN NO.	*SYMBOL*	*FUNCTION*
1	ENA	Channel A Enable Input: ENA is pulled up to VDD through a 190k resistor. If ENA is high or left open OUTA depends on INA; to disable the Channel A the ENA pin drive low regardless of the INA state
2	INA	Channel A Logic Input: INA is pulled down through a 170k resistor. OUTA is held low if INA is unbiased or floating. This pin should be connected to high state or GND (Not be left unconnected)
3	GND	Ground: Common ground reference for the device
4	INB	Channel B Logic Input: INB is pulled down through a 170k resistor. OUTB is held low if INB is unbiased or floating. This pin should be connected to high state or GND (Not be left unconnected).
5	OUTB	Channel B Output: Low impedance output with source or sink current ability
6	VDD	Supply Voltage: Provides power to the device
7	OUTA	Channel A Output: Low impedance output with source or sink current ability
8	ENB	Channel B Enable Input: ENB is pulled up to VDD through a 190k resistor. If ENB is high or left open OUTB depends on INB; to disable the channel B the ENB pin drive low regardless of the INB state

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Supply Voltage	VDD	-0.3	30	V	
Input and Enable pins Voltage	V_{INA}, V_{INB}, V_{ENA}, V_{ENB}	-10	26	V	
Output Voltage	V_{OUTA}, V_{OUTB}	-0.3	VDD+0.3	V	
		-2	VDD+3	V	Pulse<200ns
Operating Virtual Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_{STG}	-60	150	°C	

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002	±2000	V
	Charged device model (CDM), per AEC-Q100-011	±1000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Supply Voltage	VDD	5	26	V	
Input Pin Voltage	$V_{INA,B}$	-6	24	V	
Enable Pin Voltage	$V_{ENA,B}$	-6	24	V	
Operating Junction Temperature	T_J	-40	125	°C	

5. Thermal Information

Parameters	Symbol	SOP8	HMSOP8	HSOP8	Unit
Junction-to-ambient thermal resistance (1)	$R_{\theta JA}$	110	65	50	°C /W
Junction-to-case(top) thermal resistance (1)	$R_{\theta jC(top)}$	55	62	75	°C /W
Junction-to-top Characterization parameters (2)	Ψ_{JT}	18	7	16	°C /W
Junction-to-board Characterization parameters (2)	Ψ_{JB}	60	32	25	°C /W

1) Tested using High Effective Thermal Conductivity Test Board (2s2p) described in JESD51-7

2) Tested following the environment described in JESD51-2a

6. Specifications

6.1. Electrical Characteristics

Use VDD=12V, and 10uF capacitor from VDD to GND. Positive and negative symbols represents the current into and out of the specified terminal, no load to output, T_A=T_J =-40°C to 125°C (unless otherwise noted).

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
VDD Current						
Startup current	$IDD_{(OFF)}$		200		uA	VDD=3.4V, INA=INB=VDD
			180		uA	VDD=3.4V, INA=INB=GND
Quiescent current	IDD_Q		0.7	1.2	mA	ENA=ENB=VDD, INA=INB=3.3V
			0.7	1.2	mA	ENA=ENB=VDD, INA=INB=GND
Operating current	$IDD_{(op)}$		2		mA	f=500kHz
Under Voltage Lockout (UVLO)						
VDD turn-on threshold	VDD_{ON}	3.8	4.2	4.9	V	
VDD turn-off threshold	VDD_{OFF}	3.5	3.9	4.2	V	
VDD hysteresis	VDD_{HYS}		0.3		V	
Input Characteristics						
Input signal for LH transition	V_{INH}		2.3	2.7	V	Output Turns to High, If EN pin is high or left open
Input signal for HL transition	V_{INL}	0.9	1.3		V	Output Turns to low, If EN pin is high or left open
Input signal hysteresis	V_{INHYS}		1.0		V	
Enable signal for LH transition	V_{ENH}		2.3	2.7	V	Output Turns to High, If IN pin is high
Enable signal for HL transition	V_{ENL}	0.9	1.3		V	Output Turns to low, If IN pin is high
Enable signal hysteresis	V_{ENHYS}		1.0		V	
Input pull-up resistance	R_{EN}		190		kΩ	
Input pull-down resistance	R_{IN}		170		kΩ	
Output Characteristics						
Peak Source Current	I_{SRC}		5		A	t_{pulse}=200ns
Peak Sink Current	I_{SNK}		-5			t_{pulse}=200ns
Output pull-up resistance	R_{OH}		1.1	2.3	Ω	I_{OUT}=-100mA
Output pulldown resistance	R_{OL}		0.6	1.5	Ω	I_{OUT}=100mA

6.2. Switching Characteristics

Use VDD=12V, and 10uF capacitor from VDD to GND. Positive and negative symbols represents the current into and out of the specified terminal, T_A =T_J=-40°C to 125°C (unless otherwise noted).

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input to output propagation delay (1)	T_{PDLH}		19	32	ns	R_{load}=0Ω, C_{LOAD}=1.8nF, low to high transition
	T_{PDHL}		19	32	ns	R_{load}=0Ω, C_{LOAD}=1.8nF, high to low transition
Enable to output propagation delay (1)	T_{PDLH}		22	35	ns	R_{load}=0Ω, C_{LOAD}=1.8nF, low to high transition
	T_{PDHL}		22	35	ns	R_{load}=0Ω, C_{LOAD}=1.8nF, high to low transition
Rise time	T_R		9		ns	R_{load}=0Ω, C_{LOAD}=1.8nF, 20%-80%
Fall time	T_F		8		ns	R_{load}=0Ω, C_{LOAD}=1.8nF, 20%-80%
Delay matching between two channels	T_{DM}		1		ns	INA=INB, OUTA and OUTB at 50% duty cycle
Minimum input pulse width that changes the output state	T_{PW}		10		ns	R_{load}=0Ω, C_{LOAD}=1.8nF

1) See the timing diagrams in Figure 6.1

6.3. Parameters Measurement Information

Figure 6.1 shows the definition of propagation delay. Associated test circuit diagram for specification measurements is shown in Figure 6.2.

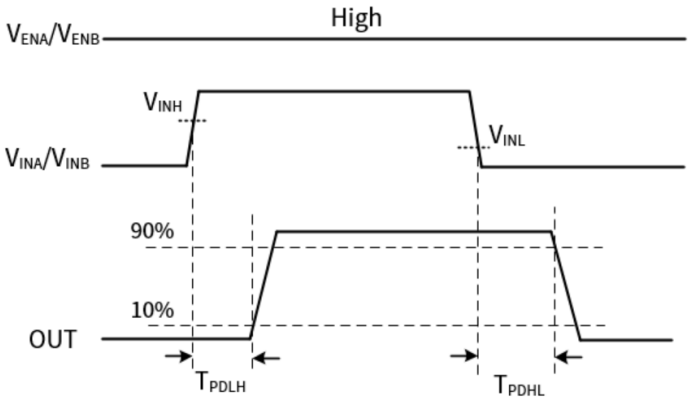


Figure 6.1 Propagation Delay

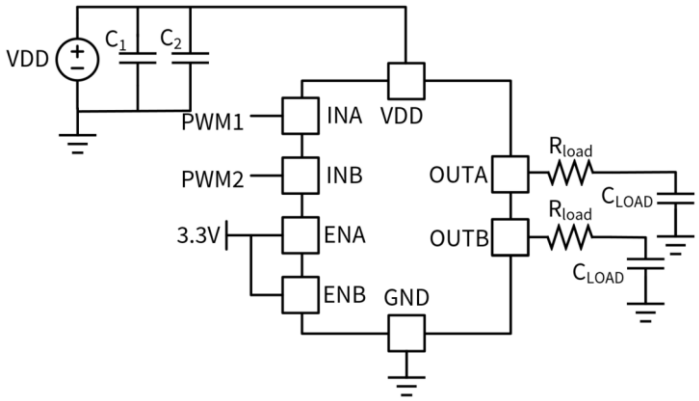


Figure 6.2 Test circuit diagram

6.4. Typical Performance Characteristics

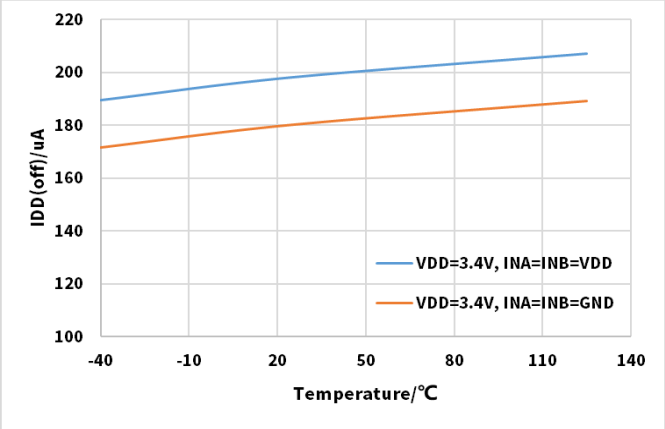


Figure 6.3 Start-up current (IDD(off)) Vs Temperature

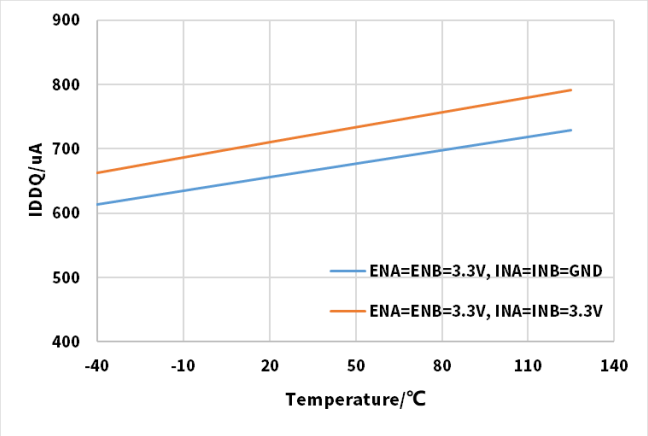


Figure 6.4 Quiescent current (IDDQ) Vs Temperature

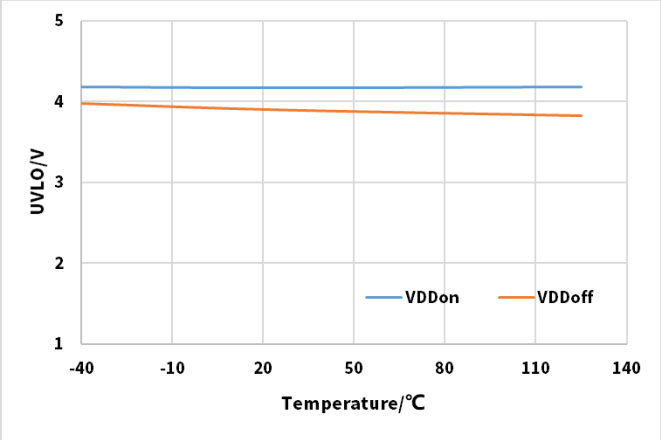


Figure 6.5 VDD UVLO Threshold Vs Temperature

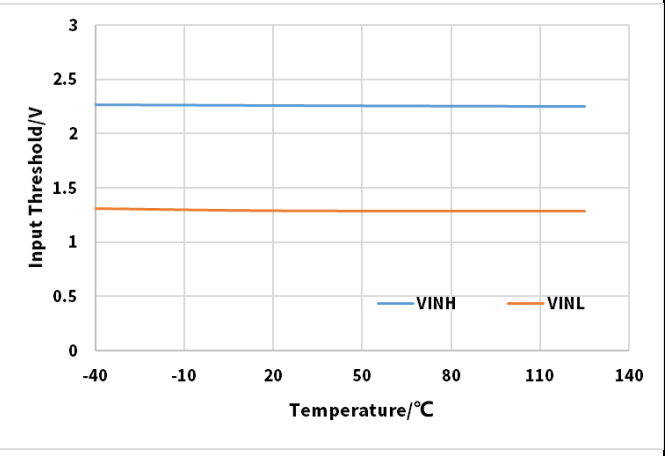


Figure 6.6 Input Threshold Vs Temperature

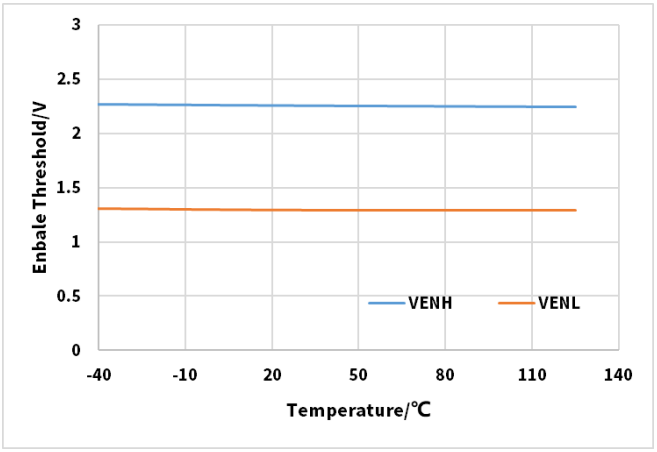


Figure 6.7 Enable Threshold Vs Temperature

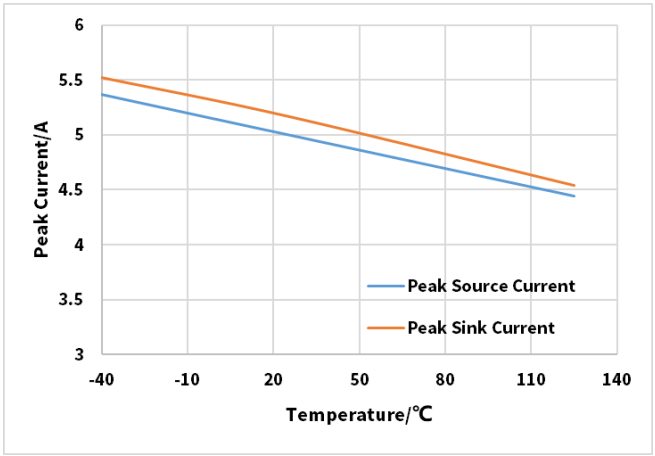


Figure 6.8 Peak Current Vs Temperature

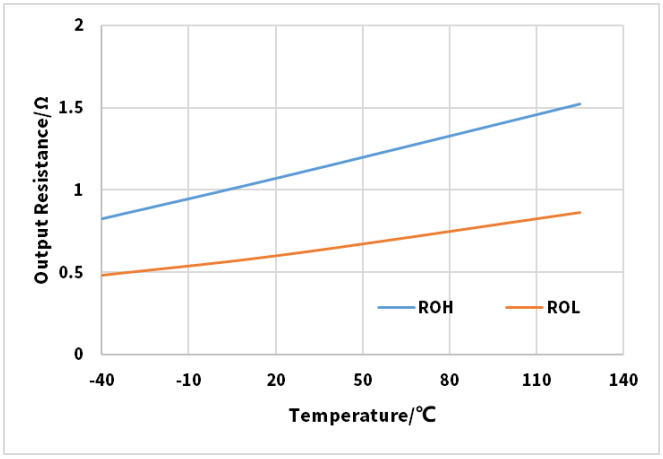


Figure 6.9 Output Resistance Vs Temperature

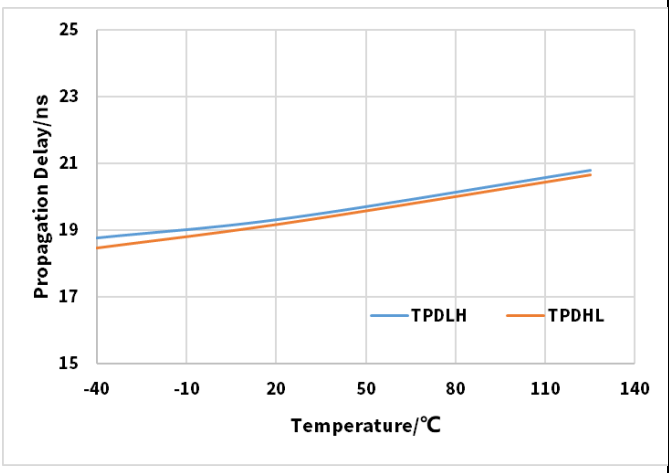


Figure 6.10 Input Propagation Delay Vs Temperature

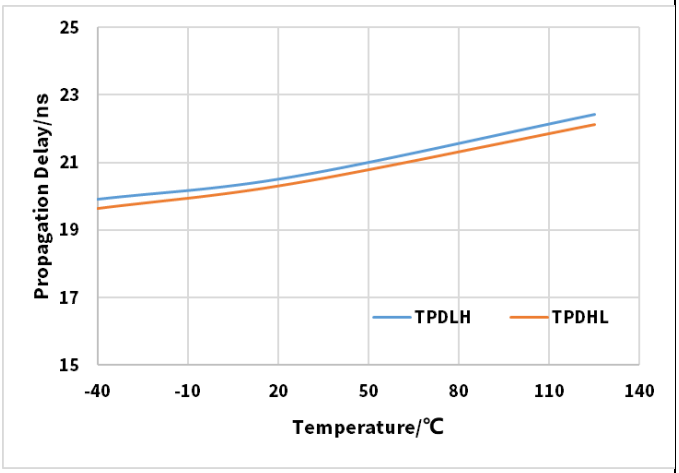


Figure 6.11 Enable Propagation Delay Vs Temperature

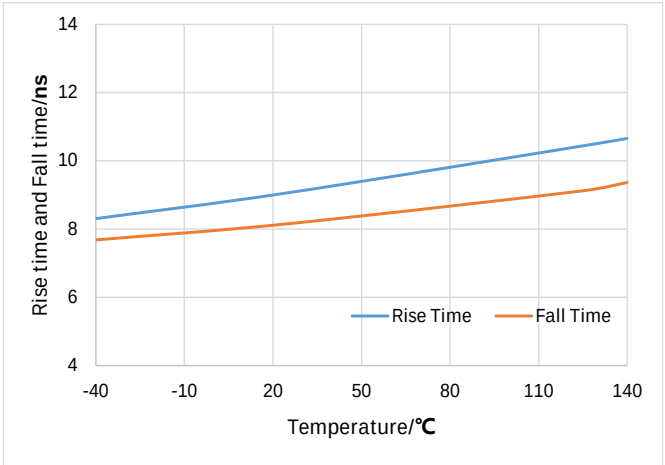


Figure 6.12 Rise and Fall time Vs Temperature

7. Detailed Description

7.1. Overview

The NSD1026V is a non-inverting high-speed dual-channel low side gate driver device featuring 5A source and sink current capability. It has capability to deliver 5A sink and source current to the capacitive load. Fast rise and fall times as well as matched propagation delay of both output channels enable the NSD1026V suitable for high frequency power converter application.

Both the input and enable pins of NSD1026V has ability to handle -10V which enhance the noise immunity of the device. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers.

The following table 7.1 ensures the efficient, robust and reliable operation in high frequency switching applications.

Table 7.1 NSD1026V Features and Advantages

FEATURE	*ADVANTAGE*
Wide range of supply voltage (VDD 5V to 26 V)	Improved the output stage robustness during switching load transition
Wide range of operating junction temperature -40 to 125°C	Flexibility in system design.
VDD UVLO Protection	Protects power MOSFETs from running into linear mode, lockout function ensures predictable, glitch-free operation at power-up and power-down
Outputs held low when input pins (INx) in floating condition	Safety feature useful in safety certification while passing abnormal condition tests
Outputs enable when enable pins (ENx) in floating condition	Independent enable pins for external control of each channel operation, PIN 1 and PIN 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Increased the noise immunity, compatible with input-logic levels from 3.3 V and 5 V microcontroller
Ability to handle -10 V (max) at input and enable pins	Enhanced the robustness in noisy conditions

7.2. Feature Description

7.2.1. Supply Voltage

NSD1026V operates under a supply voltage of 5V to 26V. The high voltage range of VDD can be useful to achieve the full current capability while driving very large MOSFETs. Two bypass capacitors from VDD to GND are recommended to get better performance and to prevent supply noise at high switching frequency. A 0.1uF surface mount ceramic capacitor must be placed as close as possible to the VDD-GND pins. Moreover, in order to prevent the unwanted glitch in the VDD supply a large capacitor of 10uF with a low ESR must be connected in parallel and close to the small value bypass capacitor.

7.2.2. Under Voltage Lockout (UVLO)

NSD1026V under voltage lockout rising threshold is typically 4.2V with 0.3V typical hysteresis. This hysteresis prevents output bouncing when low VDD supply voltage have noise from power supply. It also prevents sags in the VDD cause by sudden increase in IDD current while system commences switching. When VDD is below the UVLO threshold the circuit holds the outputs low regardless of the status of the inputs.

At power-up, the NSD1026V output remains low until the VDD reaches the turn-on threshold. The magnitude of output signal rises with VDD until it reached to steady-state value. Figure 7.1 shows that the output remains low until the UVLO threshold is reached, then the output becomes in phase with the input waveform if the EN pin is active or floating.

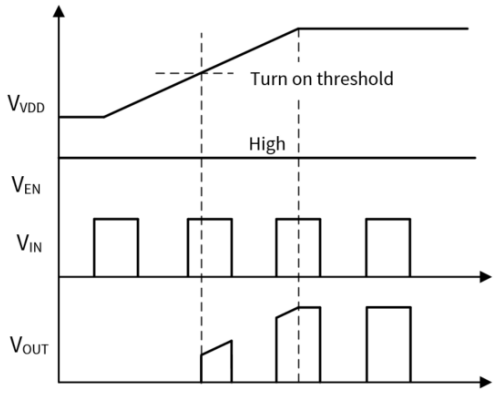


Figure 7.1 UVLO operating diagram

7.2.3. Input Stage

The input of NSD1026V is compatible to both TTL and CMOS logic threshold. The typical value of high input threshold (V_{INH} =2.3V) whereas the low threshold (V_{INL} =1.3V). The logic level thresholds are conveniently driven with PWM control signals derived from 3.3 V and 5 V digital power controller device. Wider hysteresis (typ. 1.0 V) offers enhanced noise immunity compared to traditional TTL logic implementations. NSD1026V also feature tight control of the input pin threshold voltage levels which ease system design consideration and ensure stable operation across temperature.

7.2.4. Enable Function

NSD1026V provides independent enable function for external control of each channel operation. Like the input pins, the enable pins are also based on TTL and CMOS compatible input-threshold logic and are effectively controlled using logic signals from 3.3 V and 5 V microcontroller. When the enable pin voltage reaches to high threshold (V_{ENH} =2.3V) the driver enables all functions and starts gate driver operation. Whereas, the driver operation is disabled when the enable voltage falls below its low threshold (V_{ENL} =1.3V). The enable pins are internally pulled up to VDD with 190k pull-up resistors. Therefore, the ENA & ENB pins are left floating or not connecting (NC) for standard operation, where the enable feature is not required. This driver also features tight control of the enable-function threshold-voltage levels which ease system design consideration and ensure stable operation with temperature.

All input pins have ability to handle negative voltage up to -10 V. This feature enhanced the robustness in noisy environments, and also prevent cross current over single wires during GND shift between signal source and driver input.

7.2.5. Device Functional Modes

Table 6.3 NSD1026V Device Logic

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating	H	H	H	H

8. Application Note

8.1. Typical Application Circuit

Typical synchronous rectifier and interleaved PFC power converter configuration by using the driver NSD1026V are shown in Figure 8.1 and 8.2 respectively.

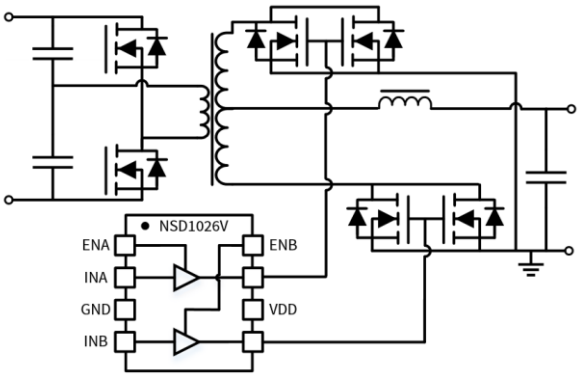


Figure 8.1 Synchronous Rectifier

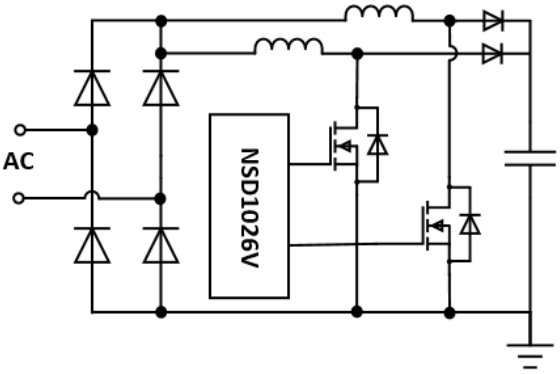


Figure 8.2 Interleaved PFC Converter

8.2. Driver Current and Power Dissipation

Power dissipation in the gate driver device for fully charged capacitive load depends on the following factors:

- Switching frequency (F_{SW})
- Supply Voltage (V_{DD})
- Load Capacitor (C_{LOAD})
- External gate resistors (R_G)

The gate charge (Q_G) includes the effect of input capacitance and the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Generally, manufacturer provides the information of gate charge, in nC, to switch the device under specified conditions. Using gate charge QG, and the power that must be dissipated during charging can be determined by the Equation 1.

$$P_G = Q_G * V_{DD} * F_{SW} \quad (1)$$

This power P_G dissipates in the gate resistor of the circuit during the MOSFET switching transitions. Half of the power dissipates when the load capacitor is charge and the other half dissipates during discharging period of the capacitor. With the use of external gate drive resistor, the power dissipation shares between internal and gate resistance of the gate driver.

By using external gate resistor R_G, the power dissipation is calculated as:

$$P_G = 0.5 * Q_G * V_{DD} * F_{SW} * \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G}\right) \quad (2)$$

Where

- R_{OL} is the effective pull down resistance
- R_{OH} is the pull up resistance
- R_G is the gate resistance between driver output and gate of power MOSFET

8.3. PCB Layout

For design robustness and proper operation at fast switching and high current applications an appropriate PCB layout design is very important. NSD1026V has ability to provide higher current (5 A peak at VDD=12 V) with very small rise and fall time at the gate of the power MOSFET to assist vary fast voltage transition. The high di/dt causes unwanted ringing, if the trace length and impedance of the loop in not well controlled. Below are the recommended guidelines to design the PCB layout of conferred high-speed gate driver.

Guidelines

- Place the driver as close as possible to the power device to minimize the output side high-current trace length
- Put the bypass capacitor (between VDD and GND) very close to the driver pins to minimize the trace length for better noise filtering. Use of SMD type devices with low ESR capacitor are highly recommended.
- For high current driving applications (in case of paralleling both channel outputs), the driver input loop of both input channels must be symmetrical to ensure the equal input propagation delay.
- In order to lower the di/dt transients all the turn-on and turnoff current loop paths must be minimized
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation
- While designing prefer to keep separate power and signal traces
- The star point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be short as possible to reduce parasitic inductance and wide as possible to reduce resistance.
- Use ground plane to provide noise shielding and thermal dissipation.

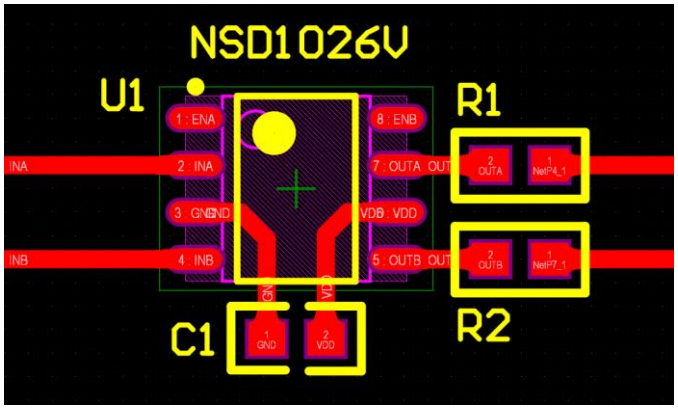
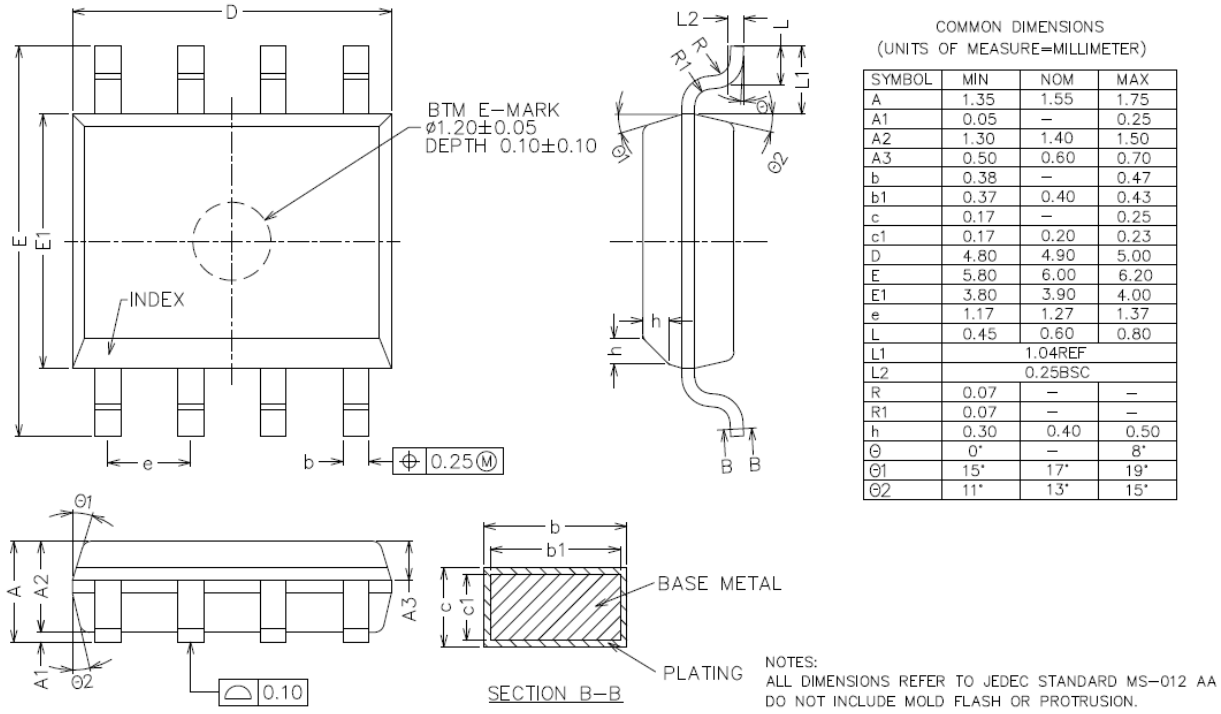


Figure 8.3 SOP8 PCB Layout example

9. Package Information

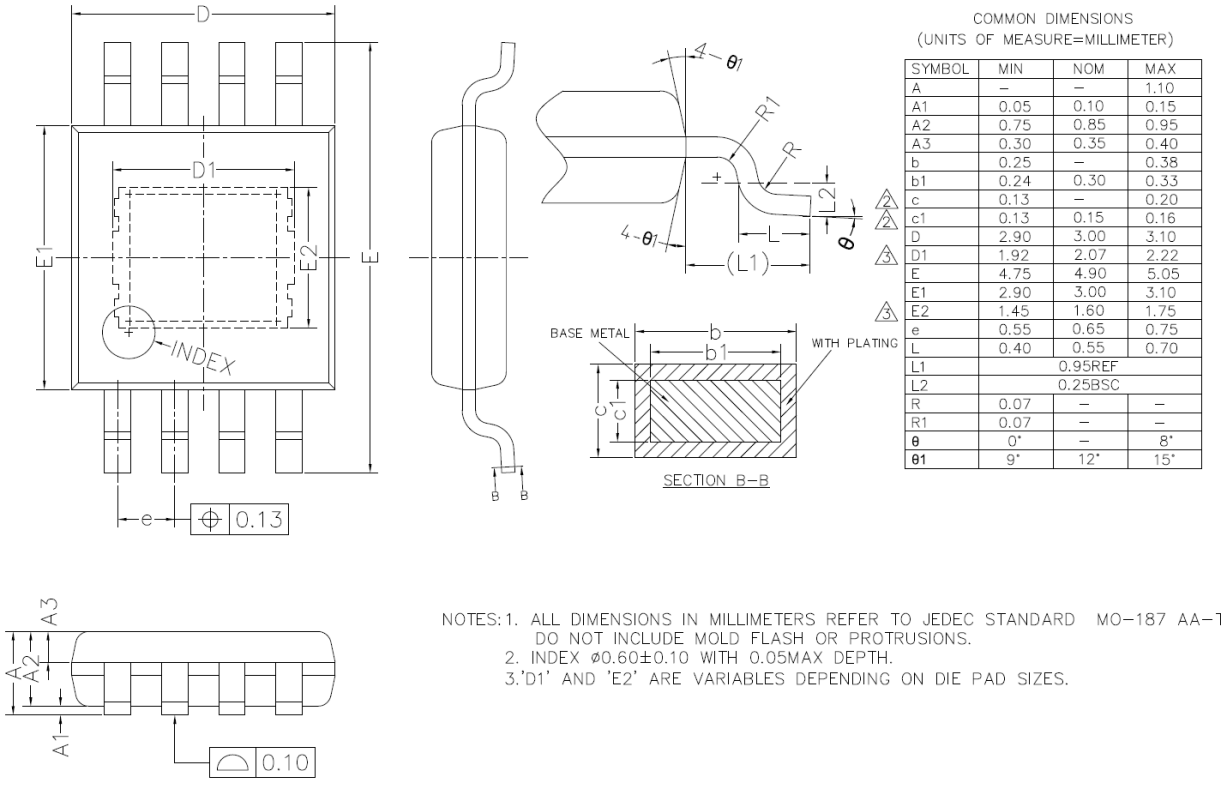


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 9.1 SOP8 Package Shape and Dimension

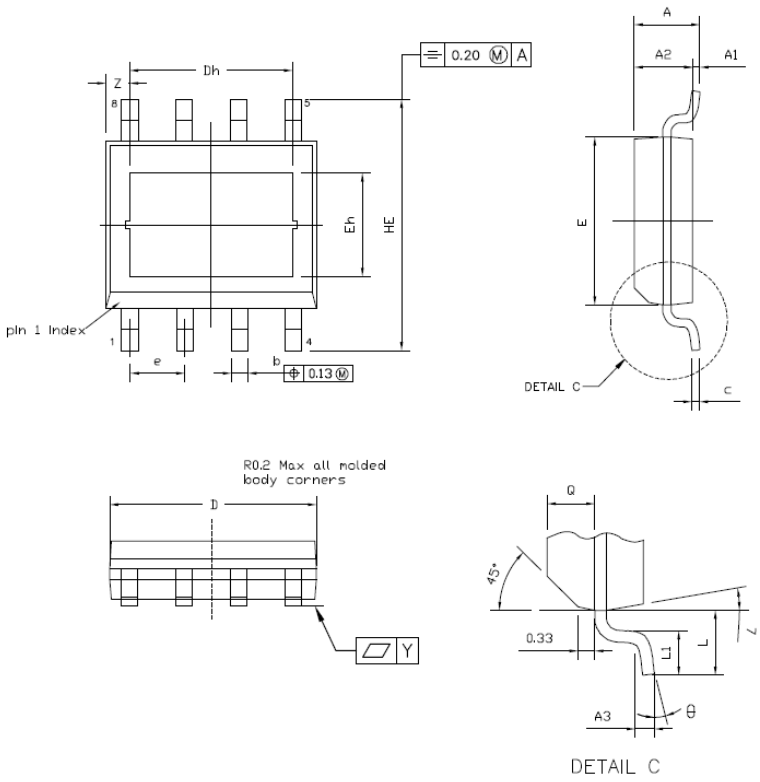


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.25	–	0.38
b1	0.24	0.30	0.33
c	0.13	–	0.20
c1	0.13	0.15	0.16
D	2.90	3.00	3.10
D1	1.92	2.07	2.22
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
E2	1.45	1.60	1.75
e	0.55	0.65	0.75
L	0.40	0.55	0.70
L1	0.95REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	9°	12°	15°

NOTES: 1. ALL DIMENSIONS IN MILLIMETERS REFER TO JEDEC STANDARD MO-187 AA-T
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX ø0.60±0.10 WITH 0.05MAX DEPTH.
3.'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

Figure 9.2 HMSOP8 Package Shape and Dimension



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.43	1.55	1.68	0.056	0.061	0.066
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	1.43	1.50	1.58	0.056	0.059	0.062
b	0.35	0.41	0.49	0.014	0.016	0.019
c	0.19	0.20	0.25	0.0075	0.0079	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.9	4.00	0.150	0.154	0.157
Q	0.55	0.65	0.75	0.022	0.026	0.030
Dh	3.71	3.81	3.91	0.146	0.150	0.154
Eh	2.19	2.29	2.39	0.086	0.090	0.094
HE	5.84	5.99	6.2	0.230	0.236	0.244
e	1.27 bsc			0.05 bsc		
L	1.05 bsc			0.041 bsc		
L1	0.41	0.64	0.89	0.016	0.025	0.035
Y	---	0.10	---	---	0.004	---
Z	0.3	0.5	0.7	0.012	0.020	0.028
A3	---	0.25	---	---	0.010	---
θ	0°	5°	8°	0°	5°	8°

Notes:
1. Package body surface finish.
   All top surface: Ra 1.2 um to 1.5 um
   All others surface: Ra 1.5 um to 1.8 um
2. LF material: CuFe2P+ESH

Figure 9.3 HSOP8 Package Shape and Dimension

10. Ordering Information

Part No.	*Temperature*	*Auto-motive*	*Package Type*	*MSL*	*SPQ*
NSD1026V-Q1SPR	-40 to 125℃	YES	SOP8	3	2500
NSD1026V-Q1HMSR	-40 to 125℃	YES	HMSOP8	3	2500
NSD1026V-Q1HSPR	-40 to 125℃	YES	HSOP8	1	2500

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSD1026V	Click here	Click here	Click here	Click here

12. Tape and Reel Information

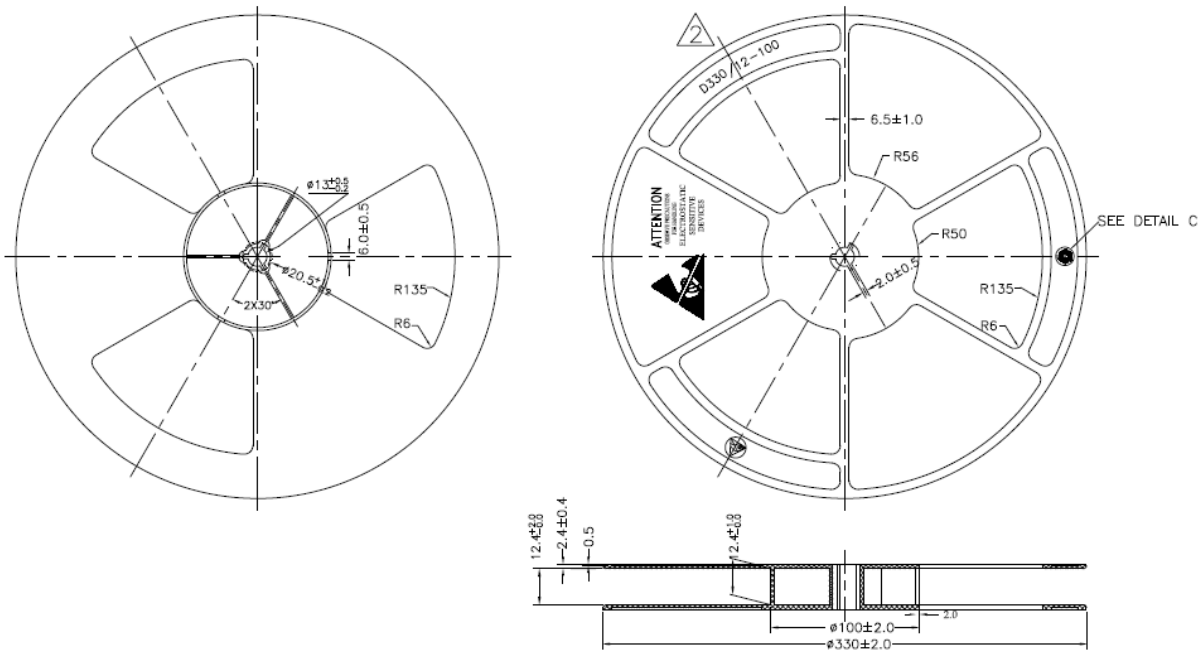


Figure 12.1 Reel information of SOP8, HSOP8 and HMSOP8

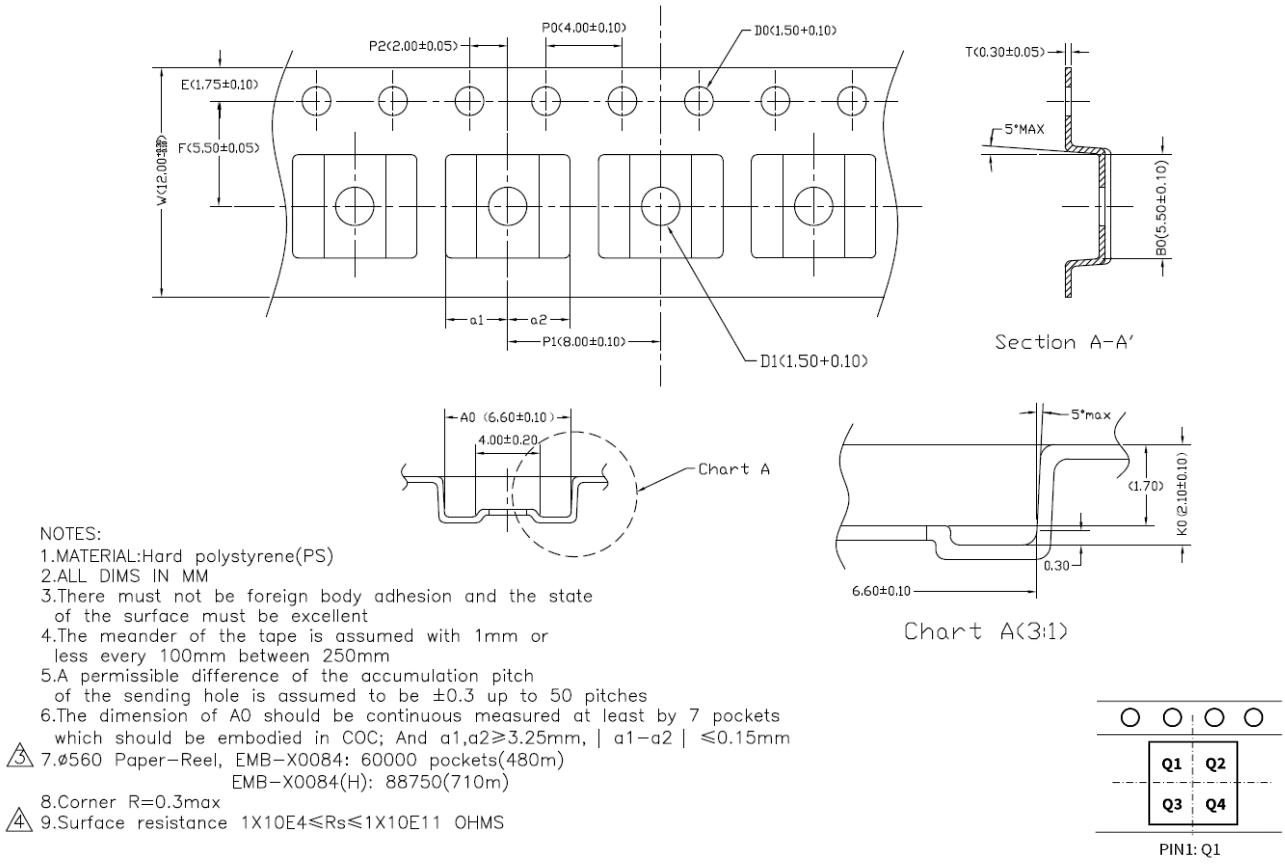
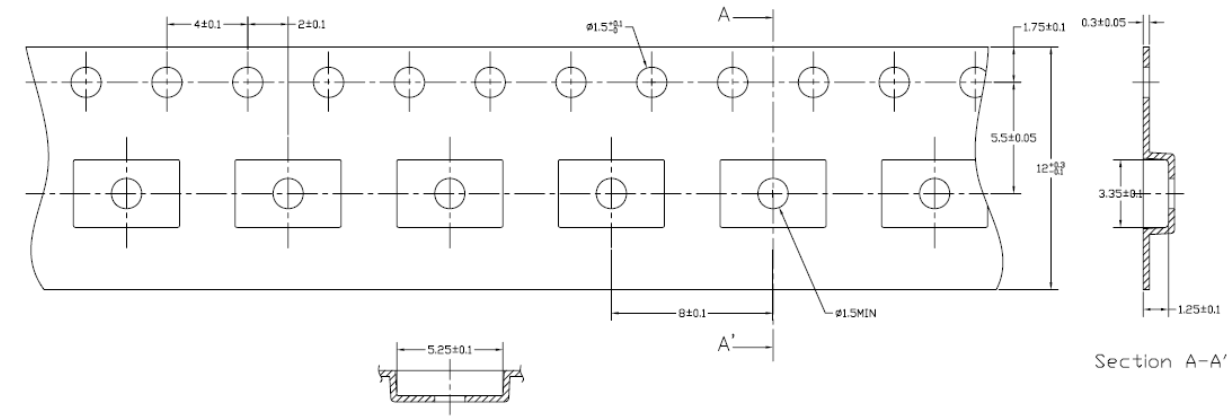


Figure 12.2 Tape information of SOP8 and HSOP8



NOTES:
1.MATERIAL:Hard polystyrene(PS)
2.ALL DIMS IN MM
3.There must not be foreign body adhesion and the state of the surface must be excellent
4.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
5.A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.3 up to 50 pitches
6.ø560 Paper-Reel, 60000 pockets(480M)
7.Corner R=0.3max
8.Surface resistance 1X10E5≤Rs≤1X10E9 OHMS/SQ

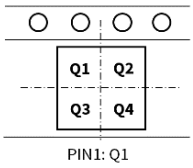


Figure 12.3 Tape information of HMSOP8

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/08/30

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