NSD5604 / NSD5604N

4-channel Low Side Driver

Datasheet (EN) 1.5

Product Overview

The NSD5604 / NSD5604N is a 4-channel low side driver for industrial and automotive applications including programmable logic control, general relays, or other solenoid drivers.

The device includes 4x parallel input interface, which controls 4x independent driving outputs for resistive, inductive, or capacitive loads. The output channels can be parallelized to support high current load and reduce device power dissipation. Low side outputs are protected against over temperature and short circuit.

The integrated diodes clamp the voltage transients generated during inductive loads turning off; combined with different external TVS connection topologies, slow decay or fast decay turn-off can be implemented.

NSD5604 also features an additional 5V max 20mA LDO output for on board digital isolator or photo coupler power supply.

Both NSD5604 & NSD5604N are available in a compact 16-pin, 4.96mm x 6.4mm HTSSOP16 package, specified over -40 to 125°C operating temperature range.

Key Features

- AEC-Q100 (Grade 1) qualified for auto-motive application
- 4x low side driver
  - Individual PWM input control interface, up to 200kHz
  - Low side driver output can be parallel
  - High speed trise and tfall
- Typical operating load current: 1 A (four channels，TA=25°C) / 2 A (one channel，TA=25°C)
- Integrated active clamping or integrated catch diodes for external Vz (clamp) pin path for inductive load fast switch off
- Wide operating ranges from 8V to 50V
- Integrated regulator 5V / 20mA output (NSD5604 version only)
- Integrated protection
  - Overcurrent / short circuit protection
  - Both common thermal and per channel over temperature protection
  - VM Input undervoltage protection
  - Dedicated nFault indicator pin
- HTSSOP16, 4.96mm X 6.40mm with exposed PAD
- RoHS& REACH Compliance

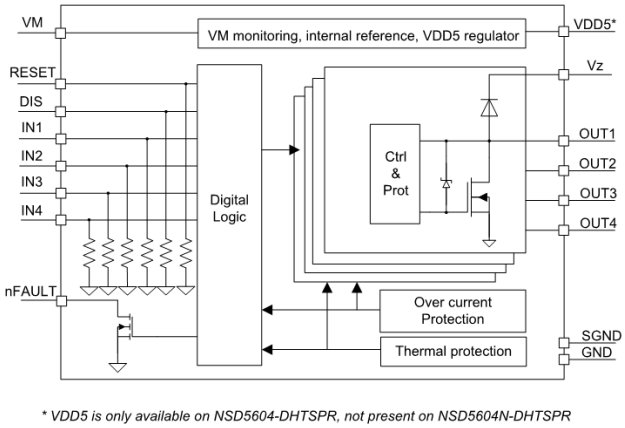
Applications

- Industrial PLCs /Automotive drivers
- General relays
- Solenoid drivers
- Unipolar stepper motor drivers

Device Information

Part Number	*Package*	*Body Size*
NSD5604-DHTSPR	HTSSOP16	4.96mm X 6.40mm
NSD5604N-DHTSPR	HTSSOP16	4.96mm X 6.40mm
NSD5604N-Q1HTSPR	HTSSOP16	4.96mm X 6.40mm

Functional Block Diagrams



** VDD5 is only available on NSD5604-DHTSPR, not present on NSD5604N-DHTSPR*

Figure 0.1 NSD5604 / NSD5604N Block Diagram

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1. Pin Configuration and Functions

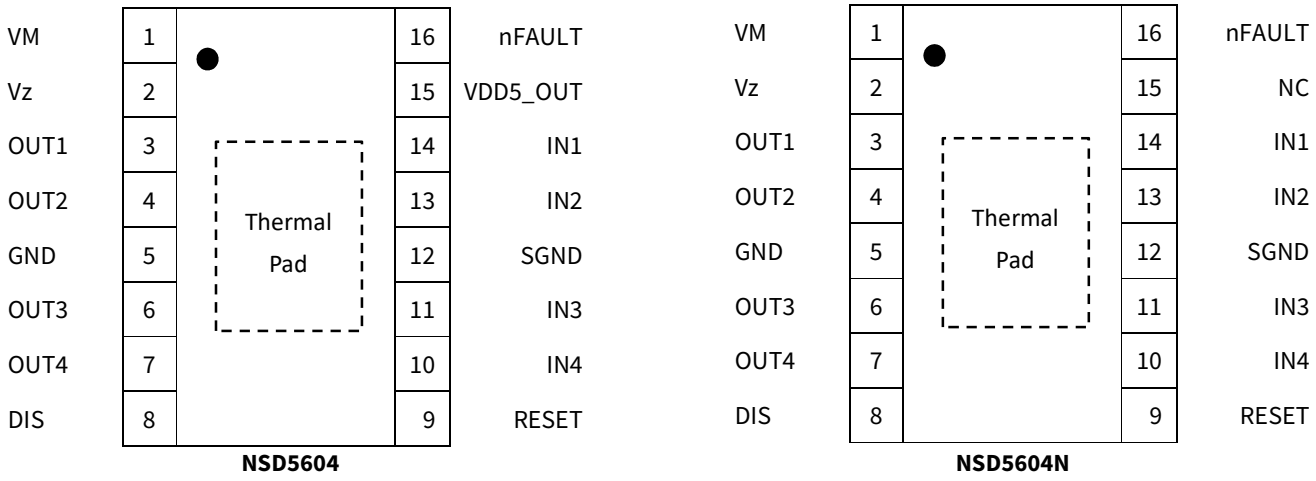


Figure 1.1 NSD5604 and NSD5604N Pinout

Table 1.1 NSD5604 and NSD5604N Pin Configuration and Description

SYMBOL	NSD5604 PIN NO.	NSD5604N PIN NO.	TYPE	DESCRIPTION
POWER AND GROUND				
VM	1		Power supply	Device power supply input.
GND	5		Power supply	Integrated power switch ground.
SGND	12		Power supply	Logic interface block ground, connect both SGND and GND to PCB ground.
VDD5	15	-	Power supply	VDD5 output pin. Recommend to place 47nF X7R ceramic capacitor close to VDD5. The function is only available on NSD5604 pinout.
NC	-	15	NC	Not connected.
CONTROL				
DIS	8		Input	Active low enables outputs, drive high to turn off all outputs.
RESET	9		Input	Drive high reset internal logic and OCP, also turn off all outputs.
IN1	14		Input	Channel 1 input, drive high to turn on low side OUT1.
IN2	13		Input	Channel 2 input, drive high to turn on low side OUT2.
IN3	11		Input	Channel 3 input, drive high to turn on low side OUT3.
IN4	10		Input	Channel 4 input, drive high to turn on low side OUT4.
STATUS				
nFAULT	16		Output	Fault output pin, open drain, logic low when in fault condition.

OUTPUT			
OUT1	3	Output	Power stage, channel 1 output.
OUT2	4	Output	Power stage, channel 2 output.
OUT3	6	Output	Power stage, channel 3 output.
OUT4	7	Output	Power stage, channel 4 output.
Vz	2	Output	Load clamp voltage pin. Connect directly to the supply rail, or by an external Zener or TVS diode to the supply rail or to PCB ground or leave it floating if not used.
Thermal Pad			
Thermal Pad	-	Power supply	Thermal pad. Must connect to board ground. For good thermal dissipation and EMC, use large ground planes on multiple layers and multiple via connecting these planes.

2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VM	Power supply voltage	–0.3	55	V
Vz	Vz voltage	–0.3	VDEMAG	V
INx, DIS, Reset, nFault	Logic input / ouput voltage	–0.3	6	V
OUTx	Output voltage	–0.3	VDEMAG	V
VDD5_OUT	VDD5 Output current	–0.3	6	V

3. ESD Ratings

SYMBOL	PARAMETER	VALUE	UNIT
VESD	Human Body Model (HBM)	±3000	V
	Charged device model (CDM)	±1000	V

4. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VM	VM Power supply voltage	8		50	V
Vz	Vz external clamp voltage	0		55	V
Reset, DIS, INx	Logic input voltage	0		5	V
fpwm	Logic input PWM frequency (INx)	0		200	kHz

5. Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	Thermal resistance, junction to case		3		°C/W
Rthja	Thermal resistance, junction to ambient, on 2-layer PCB		50		°C/W
	Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		39		°C/W

6. Electrical Characteristics

Valid for industrial version at T_j= 25°C, VM = 8 to 50V and for automotive version at T_j=-40°C to 150°C, VM= 8 to 50V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		8		50	V
I_{VM}	VM operating supply current	VM = 24V, VDD5 no load			3	mA
V_{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers	6.5		7.5	V
		VM rises until operation recovers	7		8	V
V_{UVLO_HYS}	VM undervoltage hysteresis			500		mV
t_{UVLO}	VM undervoltage deglitch time			10		µs
Regulator (VDD5_OUT only on NSD5604)						
VDD5	VDD5 output voltage	0 to 20mA load current	4.65	5	5.35	V
I_{VDD5_LIMIT}	VDD5 load current limitation	VDD5 short to GND	20		35	mA
V_{line_VDD5}	VDD5 line regulation	VM = 8V to 50V, Load current 20mA, Cvdd5 = 100nF			30	mV
V_{load_VDD5}	VDD5 load regulation	VM=24V, load current from 0mA to 20mA, Cvdd5 = 100nF			80	mV
V_{OS_VDD5}	VDD5 overshoot during power up				5.5	V

PSRR_VDD5	power supply ripple rejection	Design information f = 100kHz	40			dB
Logic Control Input (DIS, Reset, IN1, IN2, IN3, IN4)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic low current	VIN = 0 V	-5		5	μA
I_{IH}	Input logic high current	VIN = 5 V		50	100	μA
R_{PD}	Pulldown resistance	to GND		100		kΩ
$T_{Deglitch}$	Deglitch filter on DIS, Reset			2		μs
Power stage output (OUT1 / OUT2 / OUT3 /OUT4)						
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 0.5 A Ta=25°C		0.26	0.36	Ω
		VM = 24 V, I = 0.5 A Ta=125°C			0.56	Ω
Ileak	OFF-state leakage	VOUT = 24V	-10		10	μA
V_{DEMAG}	internal clamping voltage		53	58	65	V
t_{RISE}	Output rise time	VM = 24 V, OUTx rising from 10% to 90%, Resistive load	0.1	0.2	0.3	μs
t_{FALL}	Output fall time	VM = 24V, OUTx failing from 90% to 10% Resistive load	0.1	0.2	0.3	μs
t_{PD}	Propagation delay	INx to OUTx OFF->ON		0.5	0.8	μs
		INx to OUTx ON->OFF		0.5	0.8	μs
Power stage output (Vz)						
V_{FCD}	Catch diode forward voltage	VM = 24 V, I = 0.5 A		1	1.2	V
I_{RCD}	Catch diode reverse current	Vrrm = 55 V			10	μA
Current protection						

I_{OCP}	Over current threshold		2.3	3	3.8	A
t_{OCP}	Overcurrent deglitch timing			3.5		µs
t_{RETRY}	Retry timing			1.2		ms
Typical operation load current						
I_{OUT}	Continuous output current	Single channel on, Ta=25°C			2	A
		Four channels on, Ta=25°C			1	A
Thermal protection						
$T_{SD\_Central}$	Chip central thermal shutdown temperature		150	160	180	°C
$T_{SD\_Channel}$	thermal shutdown temperature		150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
nFault output						
VOL	Output low voltage	Io = 2mA			0.5	V
IOH	Output high leakage current	Vo = 5V			1	µA

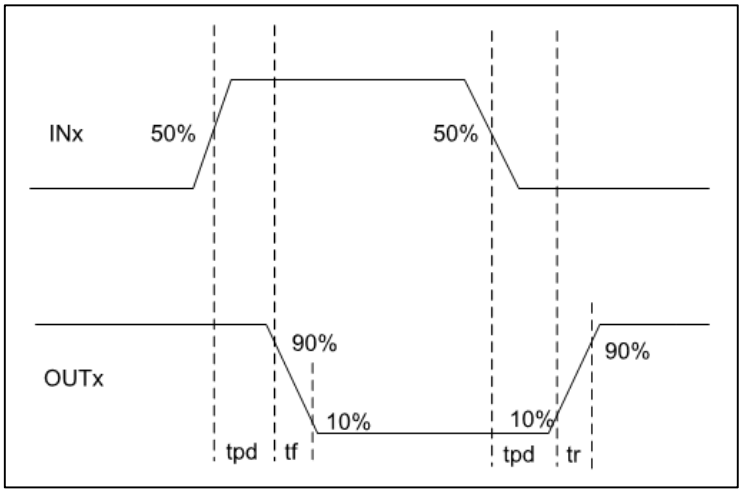


Figure 6.1 INx to OUTx propagation timing, OUTx rise timing and falling timing

7. Functional Description

7.1. VM & VM UV / OV protection

VM is the supply voltage, range from 8V to 50V with typical case 24V industrial power supply.

It is recommended to put at 1µF ceramic capacitor closed to VM pin.

When VM power supply pin voltage falls below the undervoltage threshold (V_{UVLO}) over 10µs typ. undervoltage deglitch time, low side outputs OUTx becomes OFF and internal logic are disabled. When VM rise above the V_{UVLO}, the device automatically resumes operation according to INx pin control table.

7.2. VDD5_OUT on NSD5604

VDD5_OUT pin provides stable 5V linear regulator output to external load, such as digital isolator etc. Max 20mA load current capability is supported.

Load current limitation is integrated to against overcurrent or load short to ground fault condition.

It is recommended to put 47 or 100nF X7R ceramic type capacitor on VDD5_OUT for gain regulation loop stability.

It should be noted that internal linear regulator has high power dissipation when VM in high and high load current is drawn. The power dissipation (VM-VDD5) x I_{VDD5} result the self-heating of device, for example:

VM=24V, VDD5 average load current = 15mA, P_{VDD5} = (24-5) x 0.015 = 0.135w

When NSD5604 triggers internal thermal shut down, the VDD5 regulator is automatically turn off and nFault pin asserted. Normal operation will be resumed when internal junction temperature drops below TSD-T_{HYS}, and release nFAULT pin.

Note:

VDD5_OUT is NOT allowed to work as power source which directly connecting to external load of board outside without protection.

7.3. GND, SGND and Exposed Pad

GND internally connect to the source of low side MOSFET, and it is used as power ground. SGND stands for the signal ground and provide the reference level for logic interface.

GND and SGND pins must be externally shorted on the application board.

The exposed pad at the package bottom allows better heat dissipation. It must be connected to PCB ground for best thermal performance.

7.4. Reset, DIS, IN1, IN2, IN3, IN4 Input control

INx pin accepts the ON/OFF (high/low) or PWM (max 200kHz) input signal. When it is driven high, internal logic switch on the corresponding low side output channel, vice versa, setting INx low switches off the corresponding OUTx.

Each INx input pin has typ 100kohm internal pull-down resistance.

The Reset pin signal is common for all four channels, when it is driven high, internal logic is reset and all INx inputs are ignored.

DIS pin must be low to allow output channel switch on, if DIS pin logic is set to high, all outputs switch off.

Typical 2µs filter is applied on RESET and DIS pin.

Table 7.1 RESET, DIS, INx control truth table

RESET	DIS	INx	OUTx
1	X	X	OFF
0	1	X	OFF
0	0	0	OFF
0	0	1	ON

7.5. Low side output stage, OUT1 / OUT2 / OUT3 / OUT4

The four low side drivers are designed to drive inductive/resistive/capacitive load which connects between power supply and OUTx pins.

The four power stages can be in parallel to support higher load current.

7.6. Vz pin

The device integrates internal catch diode between each OUTx and common Vz pin. It provides different decay option according to Vz pin application external connection, see section 8.2 for more details.

7.7. Protection function

7.7.1. VM undervoltage protection

When VM power supply pin voltage falls below the undervoltage threshold (V_{UVLO}) over 10µs typ. undervoltage deglitch time, low side outputs OUTx becomes OFF and internal logic are disabled. When VM rise above the V_{UVLO}, the device automatically resumes operation according to INx pin control table.

7.7.2. Overcurrent protection

In case of I_{OCP} threshold is triggered and the load current limit persists for longer than the t_{OCP} time, the low side output will be disabled and nFAULT pin driven low. The driver will remain disabled for t_{RETRY}, then the fault will be automatically cleared, and output retry to switch on if INx remains high state. See figure 4 for over current limitation behavior.

If one of four channel triggers current limitation protection, other channels remain normal operation until fault condition like common over temperature happens.

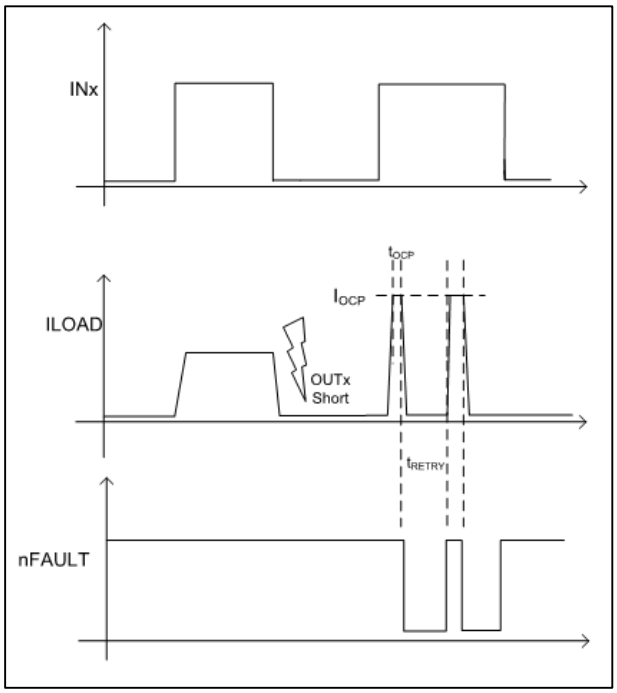


Figure 7.1 Overcurrent I_{ocp}, t_{OCP} & t_{RETRY} behavior

7.7.3. Over temperature

To protect power stage from overheat, a dedicated thermal sensor is placed close to each power MOSFET, once the sensed temperature over TSD_Channel threshold, the corresponding power MOSFET channel is automatically disabled and nFAULT pin assert low.

The thermal protection of 4x output power stages is independent.

The device also monitors die central temperature. It will disable all four power MOS and VDD5 outputs when central temperature rises above TSD_Central.

Normal operation will be resumed when the temperature drops below TSD-T_{HYS}, and release nFAULT pin.

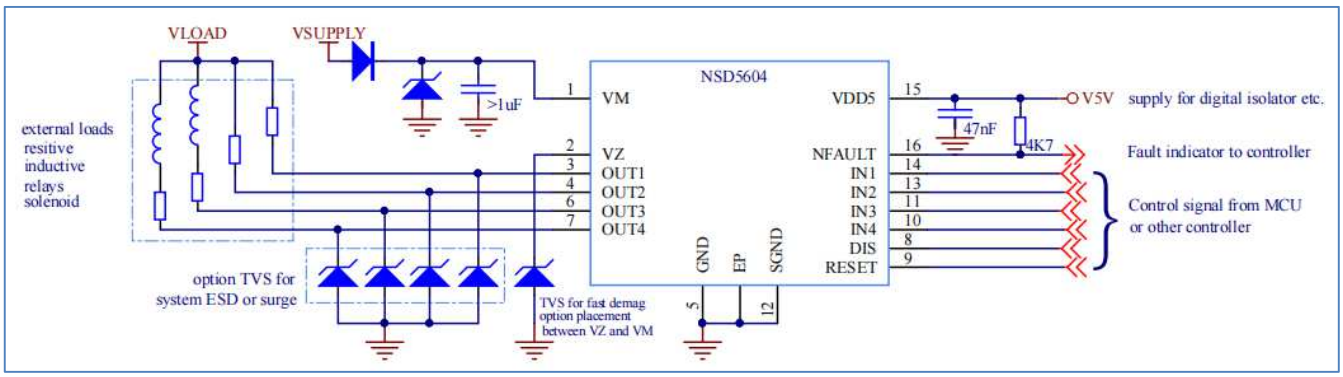
7.7.4. nFault Protection Summary

Table 7.2 nFAULT & low side behavior vs. Fault condition

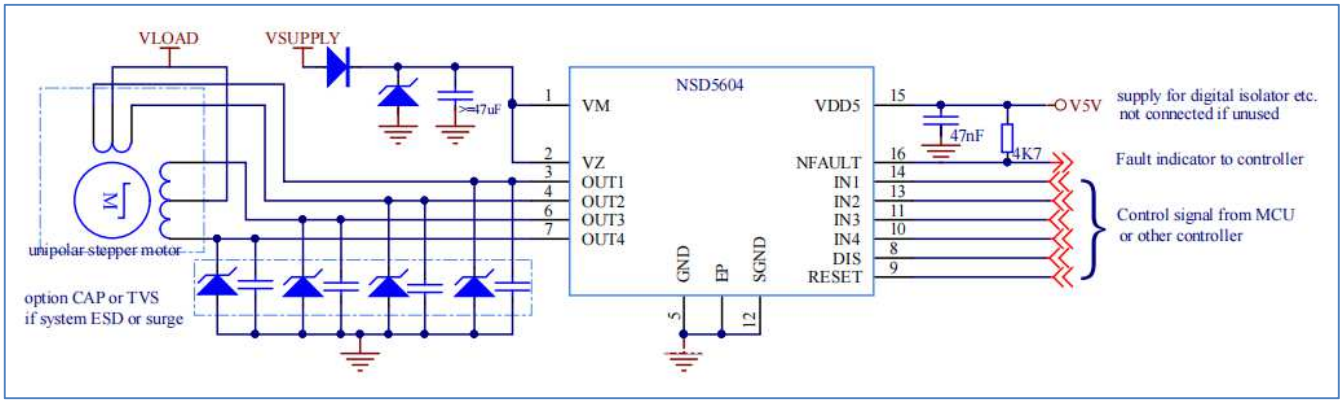
Fault	Condition	nFAULT status	Low side	Recovery procedure
VM undervoltage	VM < VUVLO	LOW	OFF	VM > VUVLO
OCP	I > Iocp	LOW	OFF	Auto retry depends on t_{OCP}, t_{RETRY} and INx
Over temperature	Low side T_J > TSD_channel or T_J> TSD_Central	LOW	OFF	TJ < TSD - THYS

8. Application information

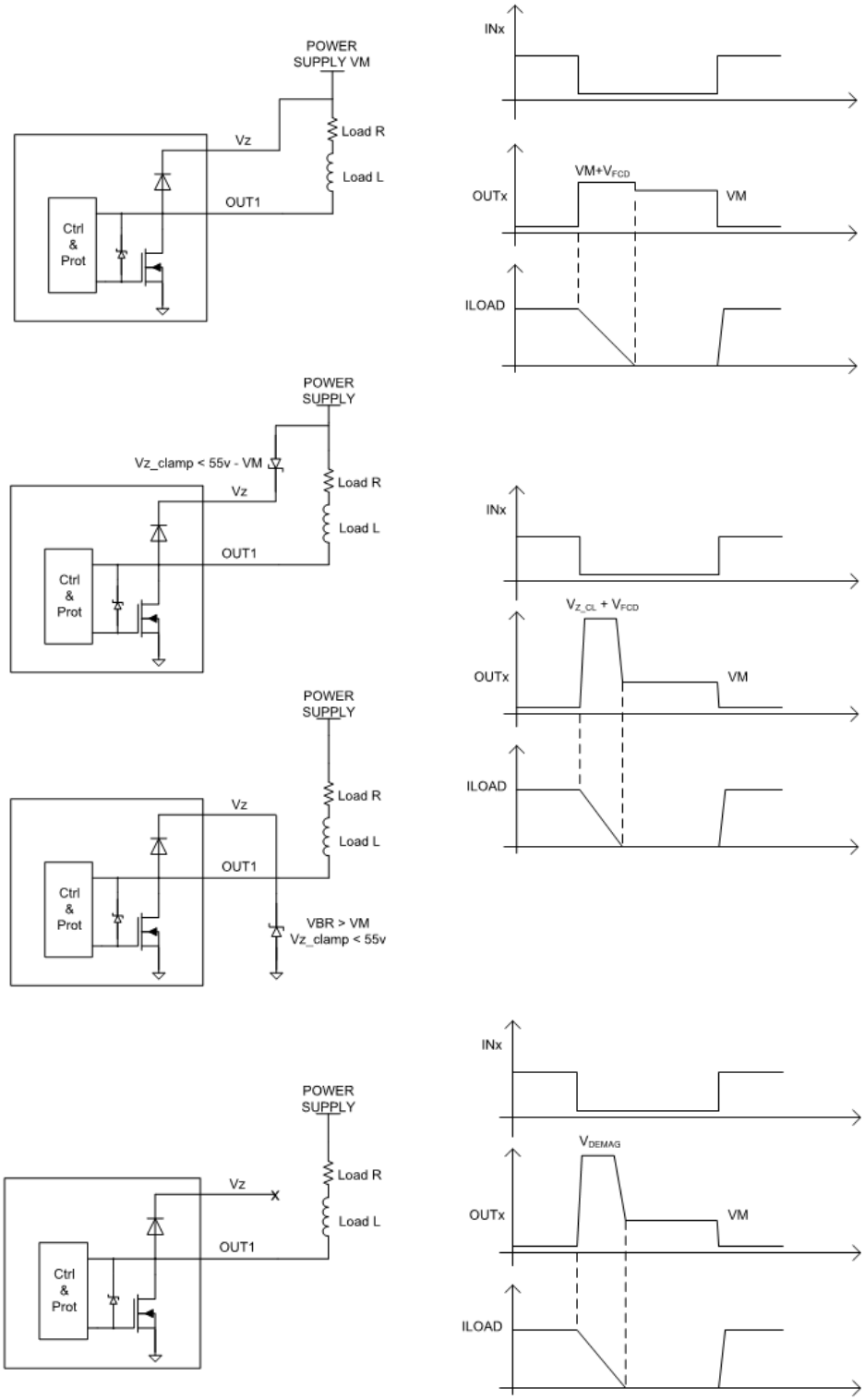
8.1. Typical circuit in PLCs or Relay application



8.2. Typical circuit in unipolar stepper motor application

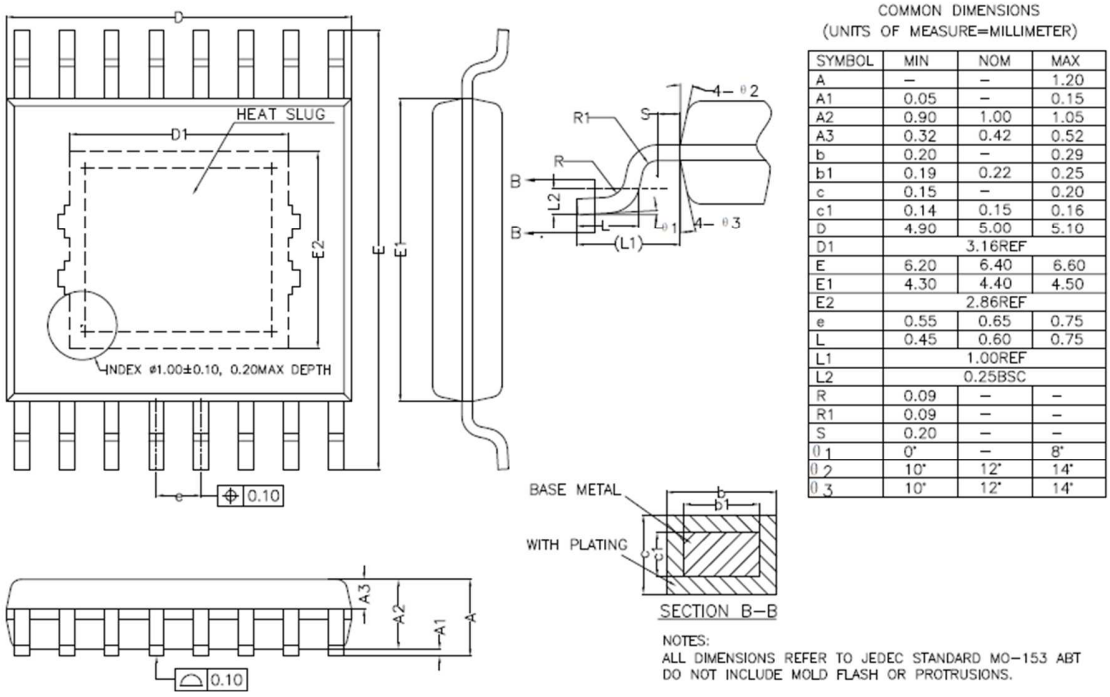


8.3. Slow decay and fast decay with external or internal active clamping



9. Package Information

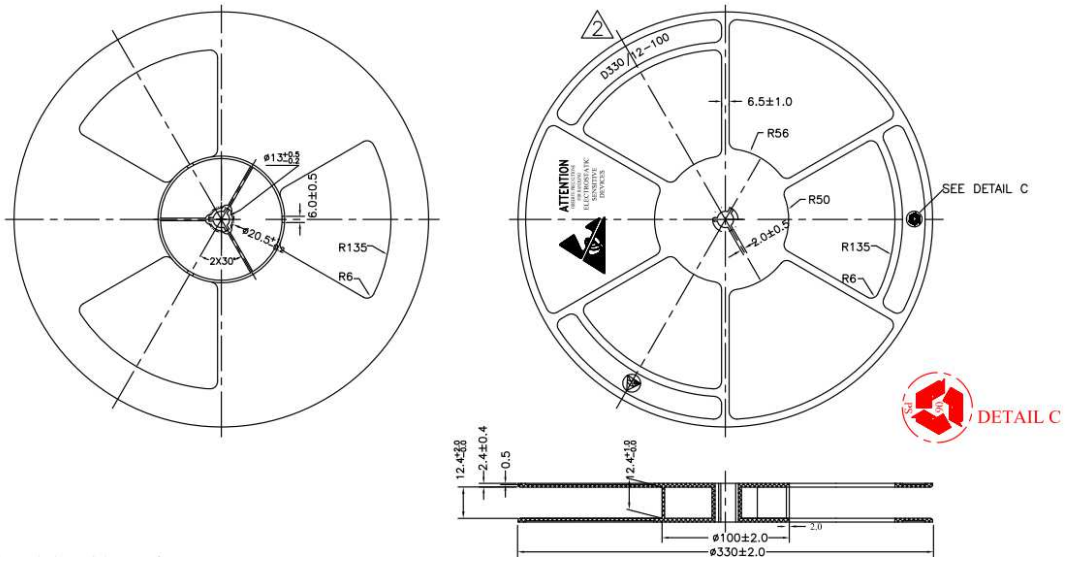
9.1. HTSSOP16 package information

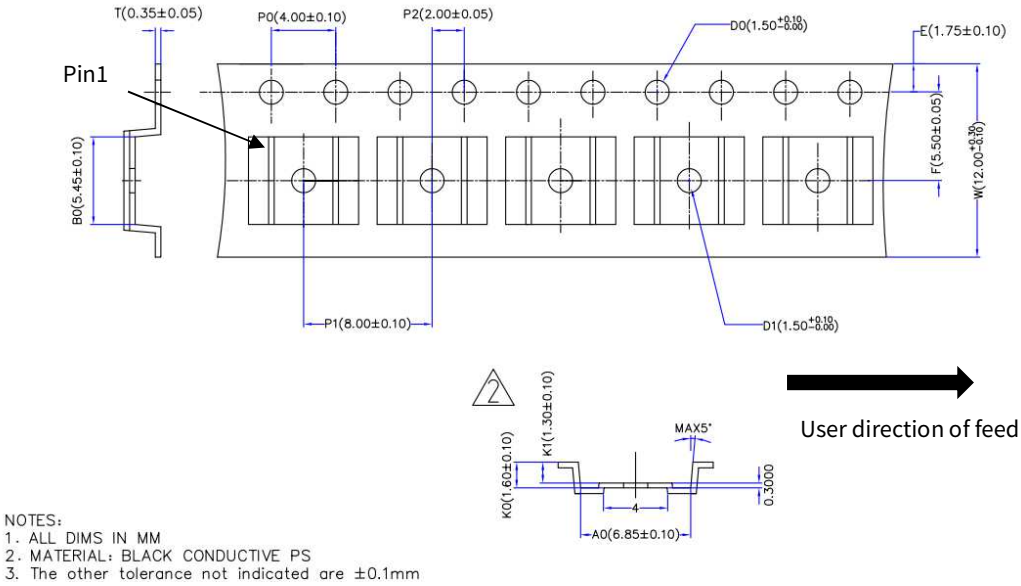


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
D1		3.16REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.86REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

9.2. HTSSOP16 packaging information





10. Ordering Information

Part Number	Automotive / Industrial	DIS / RESET	OCP	VDD5_OUT	Package Type	MSL	SPQ
NSD5604-DHTSPR	Industrial	YES	YES	YES	HTSSOP16	3	4000
NSD5604N-DHTSPR	Industrial	YES	YES	NO	HTSSOP16	3	4000
NSD5604N-Q1HTSPR	Automotive	YES	YES	NO	HTSSOP16	3	4000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.							

11. Revision History

Revision	Description	Date
1.0	Initial version	2022/12/8
1.1	Add a few max & min parameter	2022/12/28
1.2	Update output current characteristic	2023/1/19
1.3	Add automotive part number	2023/4/9
1.4	Template update	2023/8/17
1.5	Add tape reel information	2023/10/31

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