NSC9260X
Automotive Bridge Sensor Conditioner
Datasheet (EN) 1.3

Product Overview

The NSC9260X is a highly integrated and AEC-Q100 qualified IC for capacitive sensor conditioning. The NSC9260X integrates a C/V converter, a 24-bit ADC for primary signal measurement channel, a 24-bit ADC for temperature measurement channel and sensor calibration logic. With the calibration algorithm built in the internal MCU, the NSC9260X supports to compensate sensor offset, sensitivity, temperature drift up to 2nd order, and non-linearity up to the 3rd order. The calibration coefficients are stored in a 64-Byte EEPROM that can be programmed multiple times. The NSC9260X also supports Over-voltage and Reverse-voltage protection. It can provide analog output and PWM output. It can also support sensor diagnosis.

Key Features

- Over-voltage and Reverse Voltage protection between -24V ~ 28V
- Voltage supply up to 36V with an external JFET
- Directly high voltage supply up to 18V
- C/V converter with at most ±16pF differential capacitor input
- 1X~8X ADC digital gain
- 24-bit ADC for primary signal measurement
- 24-bit ADC for temperature measurement
- Sensor connection fault detection supported
- Internal and external temperature sensor supported
- Low temperature drift 16-bit DAC
- A pair of constant current sources
- Sensor calibration algorithm embedded in a built-in MCU
- 64-Bytes EEPROM
- Ratiometric or absolute voltage output
- Special OWI interface
- PWM output supported
- SSOP16 package
- Qualified according to AEC-Q100 Grade 0
- Operation temperature: -40℃~150℃
- RoHS & REACH compliance

Applications

- Capacitive Pressure sensors
- Automotive air-conditioner
- Oil Pressure sensors
- Pneumatic pressure sensors

Device Information

Part Number	*Package*	*Body Size*
NSC9260X	SSOP16	5mm ×6mm

Functional Block Diagrams

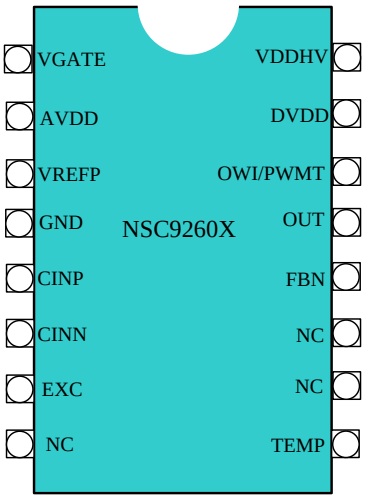

Figure 1. NSC9260X Pin Diagram

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1. Pin Configuration and Functions

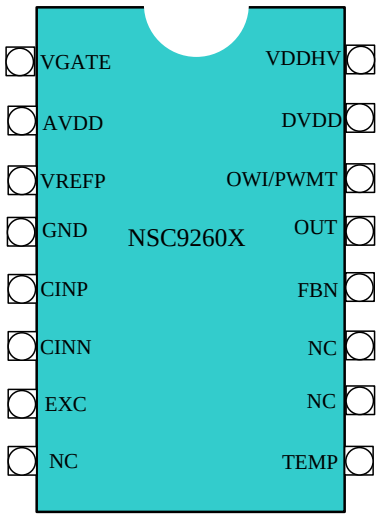


Figure 1.1 NSC9260X Pin Diagram

Table 1.1 NSC9260X Pin Configuration and Description

NSC9260X PIN No.	*Symbol*	*Function*
1	VGATE	JFET controller output
2	AVDD	Internal analog power supply
3	VREFP	Internal Reference voltage VREF output/External Reference voltage input(set by register 0xA2)
4	GND	Ground
5	CINP	Capacitance measurement channel input positive
6	CINN	Capacitance measurement channel input negative
7	EXC	Output excitation source
8	NC	Floating
9	TEMP	External temperature sensor input
10	NC	Floating
11	NC	Floating
12	FBN	Output driver feedback
13	OUT/PWMDAC	Driver output or DAC PWM output
14	OWI/PWMT	One-wire interface or Temperature channel PWM output
15	DVDD	1.8V digital supply from internal LDO
16	VDDHV	Power supply with OVP/RVP

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	$VDDHV_{max}$	-24		28	V	70℃, 1 hour
		-30		36	V	70℃, 1 minute
AVDD Output	$AVDD_{max}$	-0.3		6.5	V	
Analog Pin Voltage		-0.3		AVDD+0.3	V	
Analog Output Current Limit				25	mA	
Digital Pin Voltage		-0.3		AVDD+0.3	V	25℃
Maximum Junction Temperature	T_{jmax}			155	℃	
Storage Temperature		-60		150	℃	
Operation Temperature	T_{A_EXT}	-40		150	℃	

3. ESD Rating

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 Rev E ● All other pins to AVDD/VDDHV ● All other pins to GND ● IO pins to IO pins	±2	kV
	Charged device model(CDM), per AEC-Q100-011 Rev D ● All pins	±750	V

4. Electrical Characteristics

4.1. Electrical Characteristics

Typical conditions: VDDHV=5V; Temperature=25℃;

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage Range	VDDHV	4.5	5	5.5	V	REG_LVL=0
		5.5		18	V	REG_LVL=1
AVDD Output	AVDD		VDDHV-0.02		V	Supply on VDDHV pin, REG_LVL=0
			5.2		V	Supply on VDDHV pin, REG_LVL=1

DVDD LDO Output	DVDD	1.7	1.8	1.85	V	
Power on Reset	V_{POR_AVDD}		2.5		V	POR threshold during power-up
	V_{POR_HYS}		0.1		V	POR threshold hysteresis
Operation Current	I_{avdd1}		1.9		mA	0~5V output without resistive load (DAC_ON = 1)
Reference Voltage and Current Source						
Internal Bandgap Reference	VBG		1.200		V	Not measurable directly, proportional with VREF
VBG TC	VBG_TC		5	25	ppm/℃	-40℃~105℃
			5	30		-40℃~125℃
				45		-40℃~150℃
VREF Output	VREF		2		V	VREF_DIS=0; driven by external when VREF_DIS=1
VREF Current Limit	IVREF_limit		20		mA	Short to Ground
Capacitance Measurement Channel						
Differential Input Capacitance Range	C_{RANGE}		±16		pF	CV_RANGE<1:0> = 0'b00
			±12		pF	CV_RANGE<1:0> = 0'b01
			±8		pF	CV_RANGE<1:0> = 0'b10
			±4		pF	CV_RANGE<1:0> = 0'b11
Common Mode Capacitance Range	C_{CM_RANGE}		192/VREF		pF	CV_RANGE<1:0> = 0'b00
			144/VREF		pF	CV_RANGE<1:0> = 0'b01
			96/VREF		pF	CV_RANGE<1:0> = 0'b10
			96/VREF		pF	CV_RANGE<1:0> = 0'b11
CAPDAC Range		0		63.5	pF	0.5pF/LSB
PADC Resolution	RESRAW		24		Bits	
PADC Output Data Rate	ODR_P	5		4800	Hz	
PADC ENOB	ENOB_P	Refer to Table 6.1			Bits	Depends on ODR_P
Excitation Source (EXC)						
Excitation Frequency	CV_FREQ		38.4		kHz	CV_RANGE<1:0> = 0'b00/01
			76.8		kHz	CV_RANGE<1:0> = 0'b10/11
Excitation Voltage Amplitude	VAC		2		V	

Drivability	DRV		50		pF	Allow ground capacitance
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T		24		Bit	
TADC Gain	GAIN_T	1		4		1,2,4
TADC Output Data Rate	ODR_T	5		4800	Hz	
TADC ENOB	ENOB_T	Refer to Table 6.3				
Error of Internal Temperature Sensor			±1.5	±3	℃	-40 to 125 ℃
TEMP Input Impedance			1		Gohm	
DAC and Output Buffer						
DAC Resolution			16		Bit	
DAC Full Scale	VFSDAC	5V, 3.3V, 1.2V or Ratiometric				Depends on DAC_REF<1:0>
DAC Output RMS noise	Vrms		0.5		mV	
Output Load Resistance	Rload	1			kohm	
Output Load Capacitance	Cload			150	nF	
Output Shorted Current Limit	Ishort_lmt		20		mA	
Clamp High Level	Vclamph	0.5		1	VFSDAC	Set by CLAMP_HIGH<7:0>
Clamp Low Level	Vclampl	0		0.5	VFSDAC	Set by CLAMP_LOW<7:0>
OSC						
ADC Clock	FOSC_MOD		1.2		MHz	
Clock Rate Error	FOSC_ERR	-2%		1%		-40~125℃
EEPROM						
Programming Temperature	T_{EEP}	-40		105	℃	
Programming Supply Voltage	VEE	3		5.5	V	
Time for EEPROM Programming	T_{EEP}		0.8		s	
Endurance			10k			
Date Retention		10			A	@150℃
Serial Interface						
OWI Bit Period	Towi	0.03		4	ms	
OWI Pull-up Resistance	Rowi_pu	300			Ohm	

5. Register Description

The register map of the NSC9260X includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written by external interface on command mode (register 'CMD' = '0x00').

5.1. Normal Registers

IF_CTRL(R/W)

Addr	Bit	Register Name	Default	Description
0x00	5, 2	SOFTRESET	1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

STATUS (Read Only)

Addr	Bit	Register Name	Default	Description
0x02	7 – 3	ERROR_CODE<4:0>	5'b00000	Code error: Bit6=1: VIP open or VREF short; Bit5=1: VIP short to GND ; Bit4=1: VIN open or short to VREF; Bit3=1: VIN short to GND
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'OWI_AC_EN', 'OWI_WINDOW,' 'JFET_DIS', 'VREF_DIS', 'EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag
	0	DRDY	1'b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read Only, Primary Channel Data Register)

Addr	Bit	Register Name	Default	Description
0x06	7 – 0	PDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_P' = 1, store the ADC output of primary channel; When 'RAW_P' = 0, store the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read Only, Temperature Channel Data Register)

Addr	Bit	Register Name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_T' = 1, store the ADC output of temperature channel; When 'RAW_T' = 0, store the calibrated temperature data, LSB = 1/2^16℃. Real Temperature = TDATA/2^16+25℃
0x0a	7 – 0	TDATA<15:8>	0x00	
0x0b	7 – 0	TDATA<7:0>	0x00	

DAC_DATA (R/W, DAC Input Data Register)

Addr	Bit	Register Name	Default	Description
0x12	7 – 0	DAC_DATA<15:8>	0x00	DAC input data, unsigned; When 'RAW_P' = 0, set by the internal calibration logic, read only; When 'RAW_P' = 1, set externally through serial interface.
0x13	7 – 0	DAC_DATA<7:0>	0x00	

COMMAND (R/W, Command Register)

Addr	Bit	Register Name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: Command mode, all EEPROM can be written only in command mode; 0x03: Active mode; 0x33: Enter EEPROM program mode.

QUIT_OWI (Write Only)

Addr	Bit	Register Name	Default	Description
0x61	7 – 0	QUIT_OWI <7:0>	0x00	Write '0x5D' to this register to quit OWI communication. If 'QUIT_OWI_CNT' = 0x00, quit OWI communication permanently; If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporarily with a certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Addr	Bit	Register Name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporarily quit OWI communication Mode. 0x00: Quit forever, 0x01: 50ms, 0x02: 100ms … 0xFF: 12.8s

EE_PROG (R/W)

Addr	Bit	Register Name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '3E' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming finished.

VDD_CHECK (R/W)

Addr	Bit	Register Name	Default	Description
0x70	0	VDD_CHECK	1'b0	Write '1' to force VDD/2 as the input of temperature ADC.

5.2. EEPROM Registers

SYS_CONFIG1 (R/W)

Addr	Bit	Register Name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: One segment calibration with the 2nd order temperature coefficients; 1: Two segment calibration with the 1st order temperature coefficients
	6	BURNOUT_EN	1'b0	1: Enable the 100nA burnout current sources.
	5	FAULT_ON	1'b0	1: When any fault is detected, pull analog output to a fixed-level voltage
	4	FAULT_LVL	1'b0	1: High alarm output; 0: Low alarm output
	3	OWI_PUSHPULL	1'b0	0: OWI is open-drain with the need of pull-up resistor during communication; 1: OWI is push-pull without the need of pull-up resistor
	2	RESERVED	1'b0	RESEVED
	1	OWI_DIS	1'b0	1: OWI disabled (won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	RESEVED	1'b0	RESEVED

SYS_CONFIG2 (R/W)

Addr	Bit	Register Name	Default	Description
0xa2	7	JFET_DIS	1'b0	1: Disable JFET regulator
	6	JFET_LVL	1'b0	0: VDDHV overvoltage clamp value is 6.0V; AVDD output 5V during JFET power supply; 1: VDDHV overvoltage clamp value is 5.2V; AVDD output 3.3V during JFET power supply
	5	VREF_DIS	1'b0	1: Disable reference buffer, and reference voltage can be forced externally
	4	RESEVED	1'b0	RESEVED
	3	T_OUT_EN	1'b0	1: When not in OWI mode, TADC data outputs through OWI pin in PWM format
	2 - 0	OUT_MODE<2:0>	3'b000	000: Voltage output with external feedback; 001: Voltage output with internal feedback; 010/011/100: Reserved; 101: DAC PWM output; 110: Reserved, should not be used; 111: Disable DAC

CV_CONFIG (R/W)

Addr	Bit	Register Name	Default	Description
0xa3	7	CV_MODE	1'b0	0: Drive mode for C/V converter; 1: Ground mode for C/V converter
	6– 0	CAPOFF<6:0>	6'b000000	Set internal CAPDAC offset for input CAPOFF = CAPOFF<6:0>*0.5pF

PCH_Config1 (R/W)

Addr	Bit	Register Name	Default	Description
0xa4	7 – 6	RESERVED	2'b00	Should be 2'b00
	5 – 4	CV_RANGE<1:0>	2'b00	00: CRANGE = ±16pF, CCM_RANGE = 192/VREF; 01: CRANGE = ±12pF, CCM_RANGE = 144/VREF; 10: CRANGE = ±8pF, CCM_RANGE = 96/VREF; 11: CRANGE = ±4pF, CCM_RANGE = 96/VREF

PCH_Config2(R/W)

Addr	Bit	Register Name	Default	Description
0xa5	7 – 6	DAC_REF<1:0>	2'b00	DAC full scale reference 00: 5V, 01: 3.3V, 10: 1.2V, 11: AVDD (ratiometric)
	5 – 1	RESERVED<4:0>	5'b00000	Should be 5'b00000
	0	RAW_P	1'b0	0: Update calibrated sensor data into 'PDATA' register. 'DAC_DATA' will be set by internal calibration logic; 1: Update raw primary ADC data into 'PDATA' register after conversion, and allow DAC to be set externally

TCH_Config (R/W)

Addr	Bit	Register Name	Default	Description
0xa6	7	EXT_TEMP	1'b0	0: Internal temperature sensor selected; 1: External temperature sensor selected (TEMP pin as external temperature sensor input)
	6 – 5	GAIN_T<1:0>	2'b00	Gain for External temperature sensors; 00: 1X, 01: 2X, 10/11: 4X(only 4x for internal temperature)
	4 – 1	ODR_T	4'b0000	TADC output data rate, similar as ODR_P 0000: 4.8kHz, 0001: 2.4kHz, 0010: 1.2kHz, 0011: 600Hz, 0100: 300Hz, 0101: 150Hz, 0110: 75Hz, 0111: 37.5Hz, 1000: 20Hz (with 60Hz notch), 1001: 20Hz (with 50Hz notch), 1010: 10Hz (with 60Hz notch), 1011: 10Hz (with 50Hz notch), 1100: 5Hz (with 60Hz notch), 1101: 5Hz (with 50Hz notch), 1110, 1111: TADC disabled
	0	RAW_T	1'b0	1: Store the raw TADC output into 'TDATA' register; 0: Store the calibrated TADC data into 'TDATA' register

CLAMPH (R/W)

Addr	Bit	Register Name	Default	Description
0xa7	7 – 0	CLAMPH<7:0>	0x00	Set clamping high level, (1- CLAMPH *2^ (-9)) * VFSDAC

CLAMPL (R/W)

Addr	Bit	Register Name	Default	Description
0xa8	7 – 0	CLAMPL<7:0>	0x00	Set clamping low level, CLAMPL *2^ (-9) * VFSDAC

OFFSET0 (R/W)

Addr	Bit	Register Name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor calibration coefficient, offset at T0. LSB=1/2^15, RANGE (-1, +1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Addr	Bit	Register Name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1st order temperature coefficient of offset. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Addr	Bit	Register Name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2nd order temperature coefficient of offset. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5);
0xae	7 – 0	CTC2<7:0>	0x00	

				CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 1, LSB = 1/2^22, RANGE (-0.00781, +0.00781)

S0 (R/W)

Addr	Bit	Register Name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB = 1/2^15 (unsigned), RANGE (0, 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Addr	Bit	Register Name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1st order temperature coefficient of sensitivity. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xb2	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Addr	Bit	Register Name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2nd order temperature coefficient of sensitivity. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 1. LSB=1/2^22, RANGE (-0.00781, +0.00781)
0xb4	7 – 0	STC2<7:0>	0x00	

KS (R/W)

Addr	Bit	Register Name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient. LSB = 1/2^15, RANGE (-1, +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Addr	Bit	Register Name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient, LSB = 1/2^16, RANGE (-0.5, +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SCALE_OFF (R/W)

Addr	Bit	Register Name	Default	Description
0xb9	7 – 0	SCALE_OFF<23:16>	0x00	SCALE offset coefficient, LSB = 1/2^23, RANGE (-1, +1)
0xba	7 – 0	SCALE_OFF<15:8>	0x00	
0xbb	7 – 0	SCALE_OFF<7:0>	0x00	

SCALE_S (R/W)

Addr	Bit	Register Name	Default	Description
0xbc	7 – 0	SCALE_S<23:16>	0x00	SCALE sensitivity coefficient (unsigned), LSB=1/2^16 (unsigned), RANGE (0, 256)
0xbd	7 – 0	SCALE_S<15:8>	0x00	
0xbe	7 – 0	SCALE_S<7:0>	0x00	

T0 (R/W)

Addr	Bit	Register Name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Temperature Sensor calibration coefficient, reference temperature point, real reference temperature, REAL_T0 = T0 + 25. LSB = 1. RANGE (-128, +127)

KTS (R/W)

Addr	Bit	Register Name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Temperature Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor. LSB = 1/2^7, RANGE (-1, +1)

MTO (R/W)

Addr	Bit	Register Name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Temperature Sensor calibration coefficient, offset coefficient of external temperature sensor, MTO: LSB = 1/2^15, RANGE (-1, +1)
0xc2	7 – 0	MTO<7:0>	0x00	

KT (R/W)

Addr	Bit	Register Name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Temperature Sensor calibration coefficient: sensitivity coefficient of external temperature sensor, KT: LSB = 1/2^12, RANGE (-8, +8)
0xc4	7 – 0	KT<7:0>	0x00	

DAC_OFF (R/W)

Addr	Bit	Register Name	Default	Description
0xc5	7 – 0	DAC_OFF<15:8>	0xXX	DAC calibration coefficient: DAC offset LSB = 1/2^15, RANGE (-1, +1), written by NOVOSENSE after calibration at factory, should not be changed unless necessary
0xc6	7 – 0	DAC_OFF<7:0>	0xXX	

DAC_GAIN (R/W)

Addr	Bit	Register Name	Default	Description
0xc7	7 – 0	DAC_GAIN<15:8>	0xXX	DAC calibration coefficient: DAC gain coefficient, LSB = 1/2^16, RANGE (-0.5, +0.5), written by NOVOSENSE after calibration at factory, should not be changed unless necessary
0xc8	7 – 0	DAC_GAIN<7:0>	0xXX	

PADC_OFF (R/W)

Addr	Bit	Register Name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient: PADC offset, LSB = 1/2^23, RANGE (-1, +1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Addr	Bit	Register Name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration coefficient: PADC gain, LSB = 1/2^16, RANGE (-0.5, +0.5)
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0 (R/W)

Addr	Bit	Register Name	Default	Description
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient: reference pressure point for nonlinearity calibration, LSB = 1/2^7, RANGE (-1, 1)

SPARE (R/W)

Addr	Bit	Register Name	Default	Description
0xcf	7 – 0	SPARE1<7:0>	0x00	SPARE Register 1
0xd0	7 – 0	SPARE2<7:0>	0x00	SPARE Register 2
0xd1	7 – 0	SPARE3<7:0>	0x00	SPARE Register 3
0xd2	7 – 0	SPARE4<7:0>	0x00	SPARE Register 4
0xd3	7 – 0	SPARE5<7:0>	0x00	SPARE Register 5
0xd4	7 – 0	SPARE6<7:0>	0x00	SPARE Register 6
0xd5	7 – 0	SPARE7<7:0>	0x00	SPARE Register 7
0xd6	7 – 0	SPARE8<7:0>	0x00	SPARE Register 8

DIG_GAIN (R/W)

Addr	Bit	Register Name	Default	Description
0xd7	7–6	DIG_GAIN<1:0>	2'b00	Digital Gain Setting 00: 1X, 01: 2X, 10: 4X, 11: 8X
	5–0	RESERVED	6'b000000	

RESERVED

Addr	Bit	Register Name	Default	Description
0xd8	7-0	RESERVED	-	For NOVOSENSE INFO,customer should not erase these bits

EEPROM_LOCK(R/W)

Addr	*Bit*	*Register Name*	*Default*	*Description*
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock, set 1 and then EEPROM can't be programmed. (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	6 – 0	PARTID (read only)	7'b0000100	NOVOSENSE chip ID,customer should not erase these bits

6. Function Description

6.1. Overview

The NSC9260X is a highly integrated and AEC-Q100 qualified sensor conditioner for capacitive sensors. The chip supports Over-voltage and Reverse-voltage protection, as well as direct high-voltage power supply or high-voltage power supply through an external JFET. Analog output and PWM output are both available. The NSC9260X uses differential inputs with at most ±16pF differential input capacitance range and 76.8pF common mode capacitance range. The chip consists of five parts: the analog front-end module, the digital module, the analog output module, the power supply module and the serial interface. The block diagram of the NSC9260X is shown in Figure 6.1.

Analog front-end module includes a primary signal measurement channel with a C/V converter followed by a 24-bit ∑Δ ADC, a temperature measurement channel with also a 24-bit ∑Δ ADC, for precision sensor signal and temperature measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2^{nd} order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3^{rd} order. The configuration parameters and coefficients for calibration are stored in the EERPOM of 64 bytes.

The analog output module includes a 16-bit DAC and a flexible configurable output driver which can be configured to support analog output with several types of full-scale range and PWM output.

The power supply module includes a high-precision voltage reference, a sensor voltage driver, Over-voltage and Reverse-voltage protection block.

The NSC9260X supports OWI serial interface to do register writing and reading of configuration, calibration coefficients and data. Through the highly integrated and flexible interface, the NSC9260X only needs one wire to realize sensor calibration, field verification and full-scale range modification.

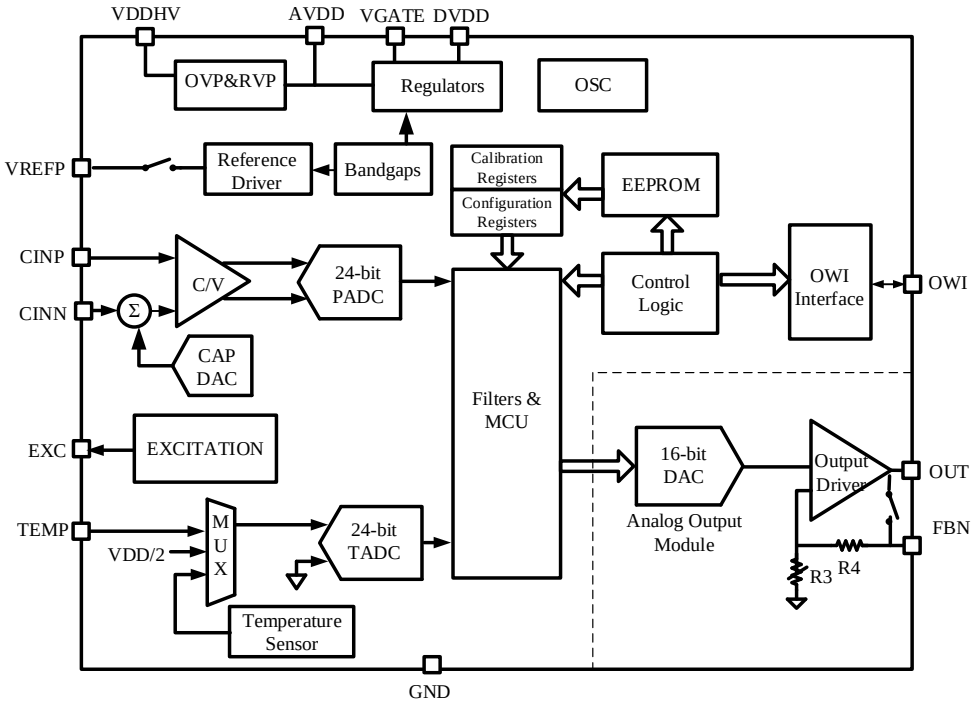


Figure 6.1 Block diagram of the NSC9260X

6.2. Analog Front-end Module 1: Primary Signal Channel

6.2.1.Capacitance Measurement Mode

The NSC9260X supports two types of capacitance measurement modes: Drive Mode and Ground Mode. The NSC9260X generates a square wave at EXC pin with frequency of 38.4kHz or 76.8kHz and VREF amplitude, which is used to drive input capacitor at Drive Mode or shield parasitic capacitor at Ground Mode.

When CV_MODE = 0, the NSC9260X is at Drive Mode, where the external input capacitors are connected as shown in Figure 6.2. The differential input capacitors' common plate is driven by the square wave at EXC pin at Drive Mode. Since the voltages at CINP and CINN keep constant, the input parasitic capacitance would not affect the output.

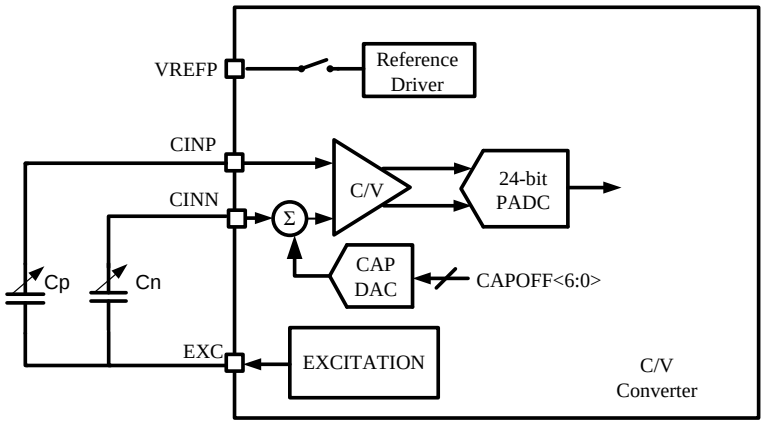


Figure 6.2 C/V converter at Drive Mode (CV_MODE = 0)

When CV_MODE = 1, the NSC9260X is at Ground Mode, where the common plate of the external differential input capacitors is grounded as shown in Figure 6.3. Both CINP and CINN are driven by the square wave at EXC pin, so the differential input capacitance is converted to voltage through charging and discharging. The 24-bit ADC then converts the voltage to digital output. Since the NSC9260X measures the capacitance between CINP/CINN and ground, the parasitic capacitance at CINP/CINN would affect the measurement directly. Even worse, the parasitic capacitance may be large and susceptible to environment interfere (such as

displacement, humidity and so on). To exclude the parasitic capacitance, CINP and CINN can be shielded with EXC pin as shown in Figure 6.3. Ground Mode is more suitable especially when the common plate of the differential input capacitors cannot be driven by the chip directly.

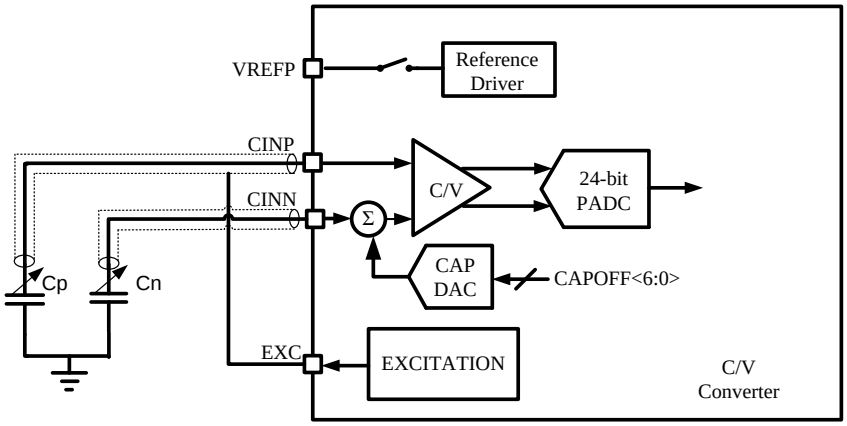


Figure6.3 C/V converter at Ground Mode (CV_MODE = 1)

6.2.2.The Measurement Range of C/V Converter

6.2.2.1.The Differential Input Capacitance Range

The PADC converts the analog output of C/V converter to digital output, which is filtered by a digital filter with 24-bit digital output $PDATA_{RAW}$. $PDATA_{RAW}$ is expressed by,

$$PDATA_{RAW} = \frac{Cp - Cn - CAPOFF}{|C_{RANGE}|} * 2^{23}$$

CAPOFF is an internal offset compensated capacitance configured by CAPOFF<6:0>. The unit capacitance of CAPDAC is 0.5pF, so it's as large as 127*0.5pF = 63.5pF. CRANGE is the full-scale range of C/V measurement configured by CV_RANGE<1:0> as referred to Section 5.1. PDATA_RAW can be read from P channel data registers (Reg0x06, 07, 08) when RAW_P = 1. When RAW_P = 0, the built-in MCU will calibrate the sensor using sensor calibration coefficients and the data of temperature measurement. Therefore, the contents of PDATA registers are the sensor output after temperature calibration.

6.2.2.2.The Common Mode Capacitance Range

When the differential input capacitance is not out of range ($PDATA_{RAW}$ is between ±1), the common mode capacitance range is expressed by

$$C_{cm} = \frac{Cp + Cn + CAPOFF}{2} < C_{cm\_range}$$

C_{cm_range} is also related to CV_RANGE<1:0> as referred to Section 5.1. In addition, C_{cm_range} is related to the VREF configuration. The smaller VREF is, the larger C_{cm_range} it supports. When much larger C_{cm_range} is required, please set VREF_DIS = 1 and drive the VREFP pin with much smaller voltage.

6.2.3.Digital Filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 4.8 kHz to 5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 6.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - log_2(RMS_{ADC})$$

RMSADC is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB (ENOBRMS) and noise free ENOB (ENOBNF) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 6.1 ENOBRMS of PADC under different ODR settings

ODR_P(Hz)	C_{RANGE}=±16pF	C_{RANGE}=±12pF	C_{RANGE}=±8pF	C_{RANGE}=±4pF
4800	15.6	15.7	16.0	15.9
2400	15.9	15.9	16.2	16.0
1200	16.3	16.2	16.7	16.6
600	16.7	16.6	17.1	17.0
300	17.1	17.2	17.6	17.4
150	17.6	17.6	18.0	17.8
75	18.1	18.1	18.5	18.4
37.5	18.6	18.6	19.1	18.7
20	19.0	19.1	19.4	19.3
10	19.6	19.5	19.9	19.8
5	20.1	20.0	20.4	20.1

6.3. Analog Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the capacitance measurement channel. The NSC9260X supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digitally filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSC9260X chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as RTD or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

6.3.1.Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers reg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSC9260X can provide a temperature reading in degree Celsius, in the format of

$$T = TDATA/2\,\hat{}\,16 + 25℃$$

For example, 'TDATA = 0x1FF24B' corresponding to 56.95 °C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 6.2.

Table 6.2 RMS noise of internal temperature sensor under different ODR_T

ODR (Hz)	2400	1200	600	300	150	75	37.5	18.75	10	5	2.5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

6.3.2.External Temperature Sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between $TDATA_{RAW}$ and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T/VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to application note. NOVOSENSE provided for calibration description details. The external temperature sensing can be done in many ways, including RTD and sensor bridge resistance itself. Figure 6.4 gives an example using a low TC drift resistor to sense the bridge resistance, which is usually proportional to the temperature of the sensor element. In case the bridge sensor is current driven, the bridge voltage can be used as temperature sensing input directly.

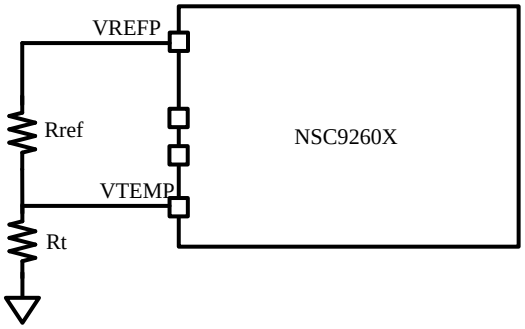


Figure 6.4 External temperature sensing using sensor bridge and a reference resistor

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 6.3.

Table 6.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T(HZ)	ENOB		
	GAIN_T = 1	GAIN_T = 2	GAIN_T = 4
4800	17.2	17.0	16.4
2400	17.6	17.4	16.7
1200	18.0	17.6	16.7
600	18.3	17.8	16.9
300	18.6	18.0	17.1
150	19.0	18.4	17.5
75	18.9	18.1	17.1
37.5	19.4	18.2	17.6
20	19.8	18.9	18.0
10	19.8	19.1	18.0
5	20.4	19.4	18.3

6.4. Analog Output Stage

The analog output stage of the NSC9260X consists of a 16-bit DAC and an output buffer with feedback network. Through register configuration and external connection, the NSC9260X provides a lot of output modes such as absolute voltage output (0~5V, 0~3.3V, 0~1.2V), ratiometric voltage output (0~AVDD), and PWM output. The output mode of analog output stage can be configured by 'OUT_MODE' registers, which is an independent configuration from analog front-end ADC.

6.4.1. 16-bit DAC

The voltage output of the DAC is expressed by the following equation,

$$VOUT = \frac{DAC\_DATA < 15:0 >}{2\,\hat{}\,16} * VFSDAC$$

'DAC_DATA' stores the DAC input data in unsigned format. VFSDAC is the full-scale range of DAC, which is configured by 'DAC_REF'. When 'RAW_P' = 0, the 'DAC_DATA' is updated by the internal MCU with the calibrated output data.

6.4.2.Analog Output Clamping

The DAC full scale range is clamped by the clamping voltage configured by 'CLAMP_HIGH' and 'CLAMP_LOW'.

The low clamping voltage is defined by the following equation,

$$VOUT\_LOW = \frac{CLAMP\_LOW < 7:0 >}{2\,\hat{}\,9} * VFSDAC$$

The high clamping voltage is defined by the following equation,

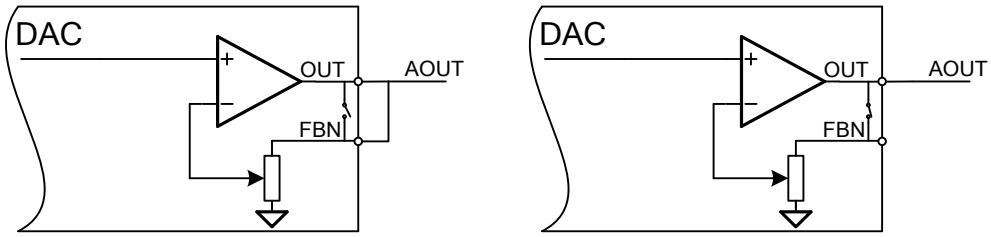
$$VOUT\_HIGH = (1\text{-}\frac{CLAMP\_HIGH < 7:0 >}{2\ \hat{}\ 9}) * VFSDAC$$

6.4.3.Voltage Output

When OUT_MODE = 000b, analog output stage is configured as voltage output mode. A class-AB output buffer is used to drive large load and the OUT pin and FBN pin should be shorted together as shown in Figure 6.5(a). The OUT pin and FBN pin can also be shorted internally as to reduce the chip pin count by setting OUT_MODE = 001b, as shown in Figure 6.5(b). The gain of output buffer is configured by 'DAC_REF' to provide several types of full-scale output range, such as absolute output (0~5V, 0~3.3V, 0~1.2V) and ratiometric output (0~AVDD), as listed in Table 6.4. The internal bandgap reference is used for absolute output.

Table 6.4 'DAC_REF' and output mode

DAC_REF<1:0>	*Output Mode*	*Output Voltage Range*
2'b00	Absolute	0~5V
2'b01	Absolute	0~3.3V
2'b10	Absolute	0~1.2V
2'b11	Ratiometric	0~AVDD



(a) External Feedback (b) Internal Feedback

Figure 6.5 Configuration for voltage output mode

If Over-voltage or Reverse-voltage happens at AOUT pin, it can be protected with external feedback as shown in Figure 6.6. The OUT pin and FBN pin are connected to AOUT through 100 ohm and 1kohm resistor respectively.

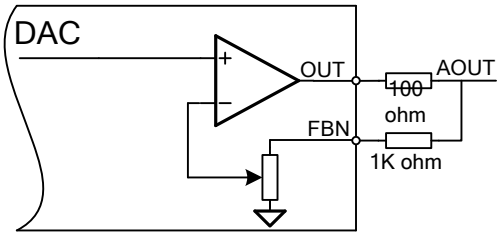


Figure 6.6 Configuration for voltage output mode with output protection

6.4.4.PWM

Both primary signal channel and temperature measurement channel support PWM output.

When 'OUT_MODE' = 101b, primary channel output data will present on the OUT pin in the PWM format. The PWM carrier frequency is fixed at 600Hz, and the PWM output duty cycle is decided by DAC_DATA<15:4> with 12-bit resolution,

PWM Duty Cycle of Primary Channel = DAC_DATA[15:4]/4096

When 'TOUT_EN' = 1 and the chip is not in OWI mode, the OWI pin is used as the output pin for Temperature Channel data in PWM format and the PWM output duty cycle is defined below:

PWM Duty Cycle of Temperature Channel = TDATA<23:12>/4096

6.5. Power Management and Sensor Drive

The NSC9260X internally includes a precision bandgap reference with very low temperature drift, less than 0.2% during full temperature range (-40~125°C). This reference voltage is used in the constant voltage or current driving circuits for clock generator and ADC/DAC etc.

6.5.1. Internal LDO

A 1.8V LDO is integrated in the NSC9260X to provide power supply for the internal digital circuits. A 100nF decoupling capacitor should be connected at DVDD pin externally.

6.5.2. Power on Reset

A POR block is integrated in the NSC9260X for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD>2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, i.e. the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

6.5.3. Over-voltage and Reverse Voltage Protection

The NSC9260X integrates an Over-voltage and Reverse-voltage Protection on power supply. Over-voltage as high as 28V and Reverse-voltage as low as -24V are allowed.

6.6. Build-in MCU Core and Control Logics

6.6.1. Work Modes

Two Different work modes are supported by the NSC9260X, command mode and active mode, which can be configured by the register 'CMD' (Reg0x30).

6.6.1.1. Command Mode

The command mode can be entered by writing the register 'CMD' with 0x00, which is used for configuring the chip outside. All the EEPROM registers (from Reg0xA1 - Reg0xD9) can only be modified only in this mode.

6.6.1.2. Active Mode

The active mode is the default mode after powering up, which can also be entered by writing the register 'CMD' with 0x03. In this mode, the primary measurement channel and the temperature channel continuously update their measured values into the 'PDATA' or 'TDATA' registers, and the selected output mode will be activated simultaneously. When the register bit 'RAW_P/T' = 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly; otherwise, every time the primary measurement channel ADC conversion ends, the built-in MCU core performs once sensor calibration flow with the latest temperature value measured.

The shadow registers inside the NSC9260X can also guarantee a non-glitch reading by keeping the 'PDATA' and 'TDATA' registers stable during once serial interface reading. Note that, the multiple bytes of one measured data should be read out together in one multi-byte serial interface reading command.

6.6.2. EEPROM

64 bytes EEPROM is contained in the NSC9260X to store the chip configurations and sensor calibration coefficients.

6.6.2.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after powering up or soft-reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set and the analog output state will be decided according to the fault diagnostic and alarm configurations. Another status register bit 'LOADING_END' will be set after the loading completes.

6.6.2.2. Programming

EEPROM registers will not be programmed into the EEPROM directly after OWI writing. The contents of the EEPROM registers will be programmed into the EEPROM by following sequence:

1.Set the register byte 'COMMAND' (Reg0x30) with 0x33 to enter EEPROM programming mode;

2.Writing the register byte 'EE_PROG' (Reg0x6A) with 0x3E to start EEROM programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to

indicate the programming is done. A re-powering up or soft-reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

6.6.2.3. Lock and Unlock

The EEPROM inside the NSC9260X can be locked by setting the 'EEPROM_LOCK' bit and programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

6.6.3. Built-in MCU Core

The NSC9260X is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

6.6.4. Calibration

The calibration inside the NSC9260X is divided into two parts. The first is the DAC calibration, which can lower the offset and sensitivity error induced by the DAC block. The second is sensor calibration, which can compensate sensor offset, sensitivity, temperature drift up to 2^{nd} order , and non-linearity up to the 3^{rd} order. The algorithm calibration error can be less than 0.1% of the full span. Please refer to application note NOVOSENSE provided.

6.7. Alarm

Configured with high clamping and low clamping registers, the NSC9260X can alarm the following external connection errors and detect if the sensor output is out of range:

- Output short to VDD
- Output short to GND
- GND open (with pull-up resistor)

The NSC9260X is protected during the following abnormal conditions: Reverse Polarity between VDDHV and GND, Reverse Polarity between OUT and GND, Reverse Polarity between OUT and VDDHV.

7. Serial Interface

The OWI serial interface is supported in the NSC9260X to configure registers, program EEPROM and read measured data. When register bit 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is defined as the OWI entering window. If a specific 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters analog output mode (as shown in Figure 7.1).

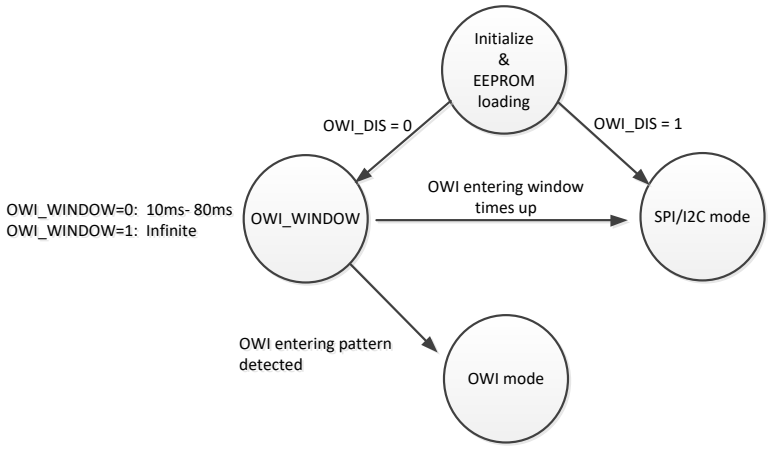


Figure 7.1 Definition of serial communication mode

7.1. OWI Pin Configuration

The OWI pin can be configured as open-drain or push-pull output by setting register 'OWI_PUSHPULL'. When 'OWI_PUSHPULL' = 0, OWI pin is open-drain output with the need of a pull-up resistor. When 'OWI_PUSHPULL' = 1, OWI pin is push-pull output.

7.2. Timing Spec

Table7.1 OWI Timing Spec

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{period}	OWI bit period		30		4000	μs
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	μs
t_{stop}	Stop condition time		2			t_{period}

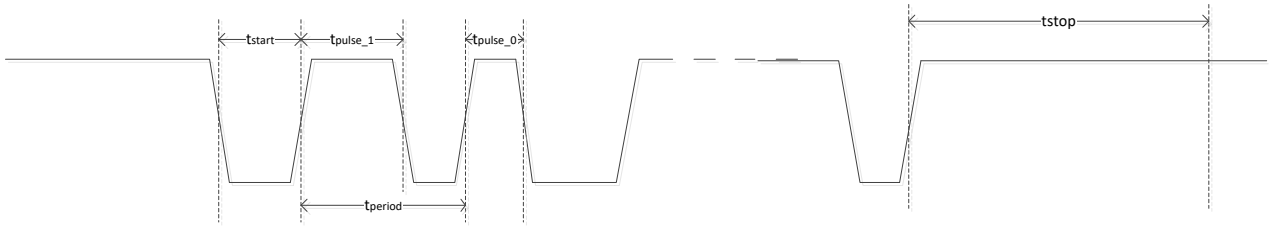


Figure 7.2 OWI Timing

7.3. Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C0, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite, the OUT pin is activated during OWI window and OWI mode, and the OWI pin and OUT pin cannot be shorted together.

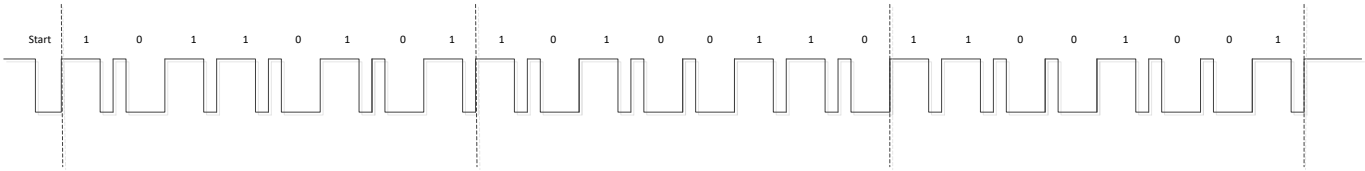


Figure 7.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

7.4. OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between 20s to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line to reach a constant high or low voltage level for at least two times of the bit period (tBperiod).

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number and a read/write–bit (0-write, 1-read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1byte, 01: 2bytes, 10: 3bytes, 11: 4bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

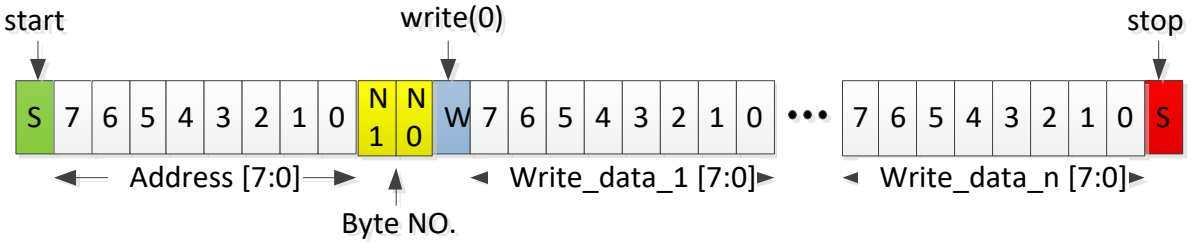


Figure 7.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is the content in the addressed register and following ones. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0,

C1 = Read_data [7] ^ Read_data [5] ^ Read_data [3] ^ Read_data [1];

C0 = Read_data [6] ^ Read_data [4] ^ Read_data [2] ^ Read_data [0].

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

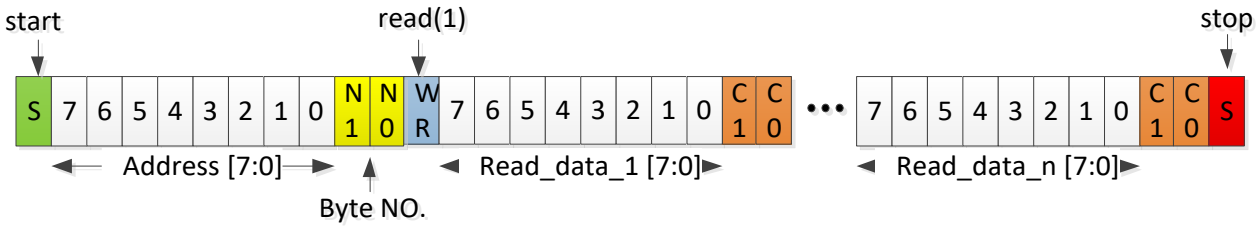


Figure 7.5 OWI Read Operation

7.5. Quit OWI Communication

Writing Reg0x61 with 0x5d during OWI mode can temporarily or permanently quit the OWI communication for output voltage or current measuring. The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 50ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

8. Application Note

8.1. Typical Application Circuit1

The application circuit of a capacitive sensor at Drive Mode is shown in Figure 8.1, where OUT pin has Over-voltage and Reverse-voltage Protection.

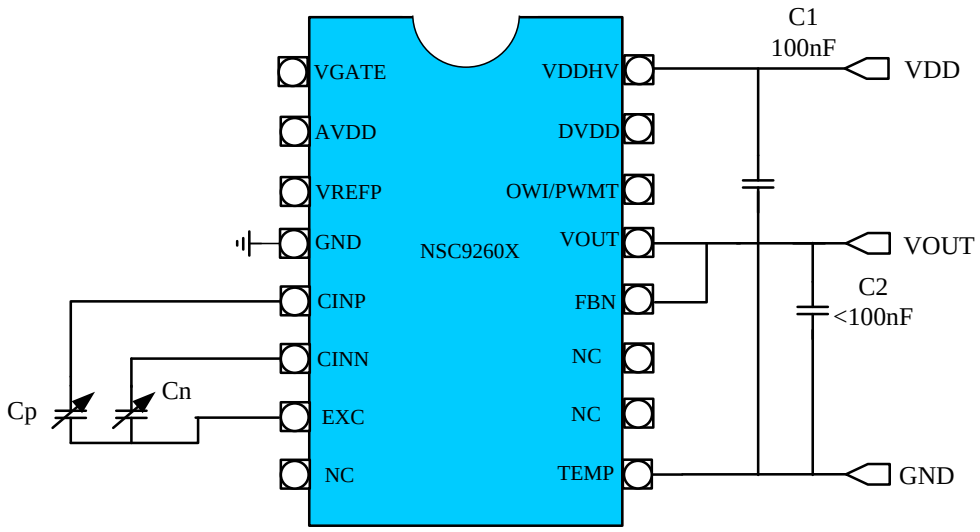


Figure 8.1 Absolute/ratiometric voltage output with Over-voltage Protection

8.2. Typical Application Circuit2

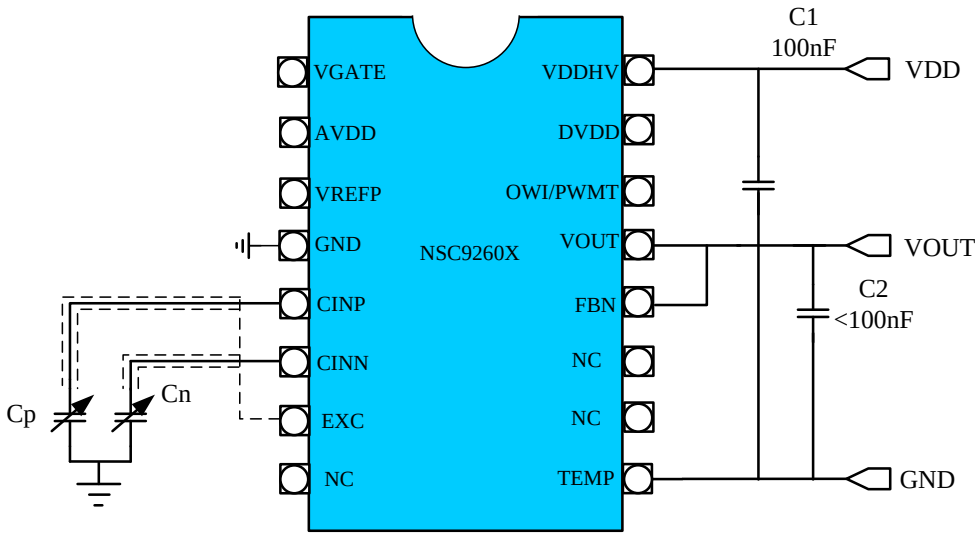


Figure 8.2 Capacitive sensor at Ground Mode with PWM output

8.3. Typical Application Circuit3

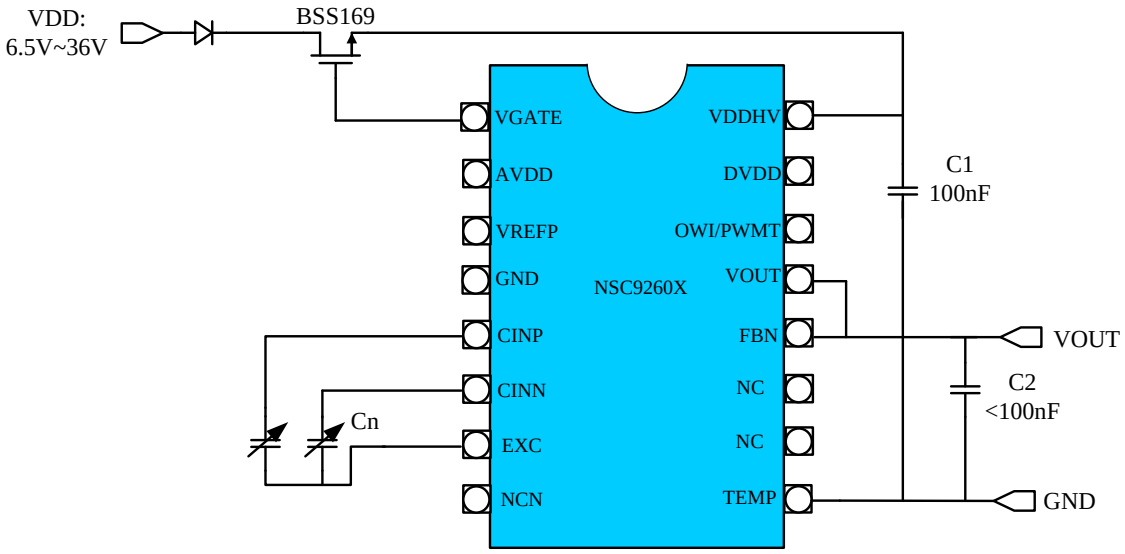


Figure 8.3 0~5V voltage output mode with external JFET regulator

8.4. Typical Application Circuit4

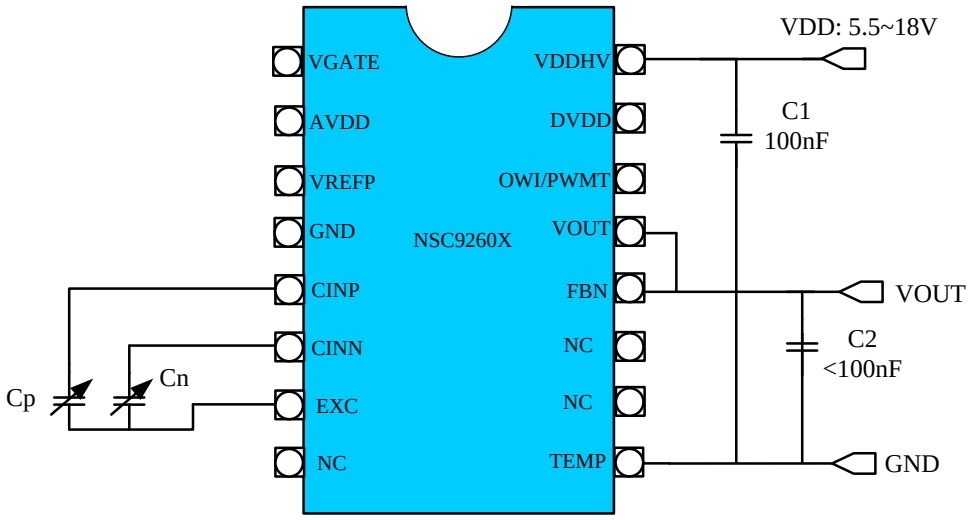
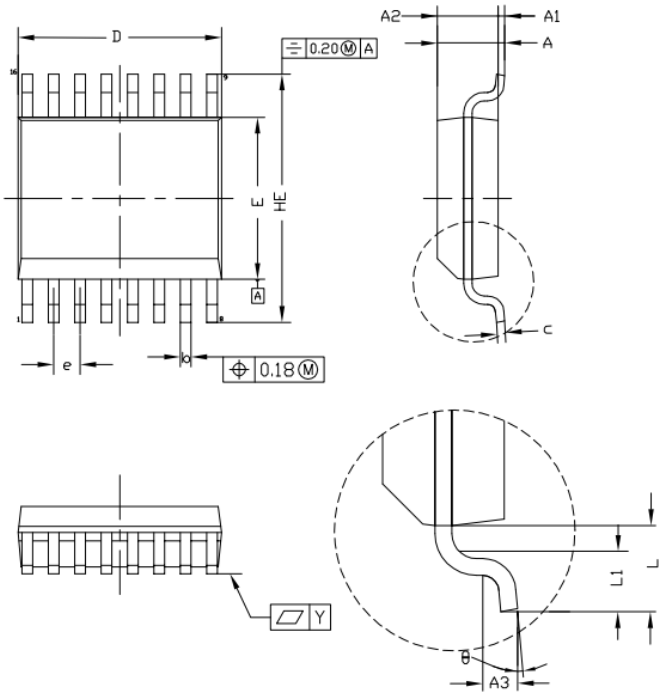


Figure 8.4 0~5V voltage output mode with high voltage directly supplied on VDDHV

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 9.1 SSOP16 package shape and dimension

10. Ordering Information

Part Number	*Temperature*	*Vehicle specification level*	*MSL*	*Package Type*	*SPQ*
NSC9260X-QSSR	-40 to 150℃	AEC-Q100 Grade 0	1	SSOP16	2500

11. Tape and Reel Information

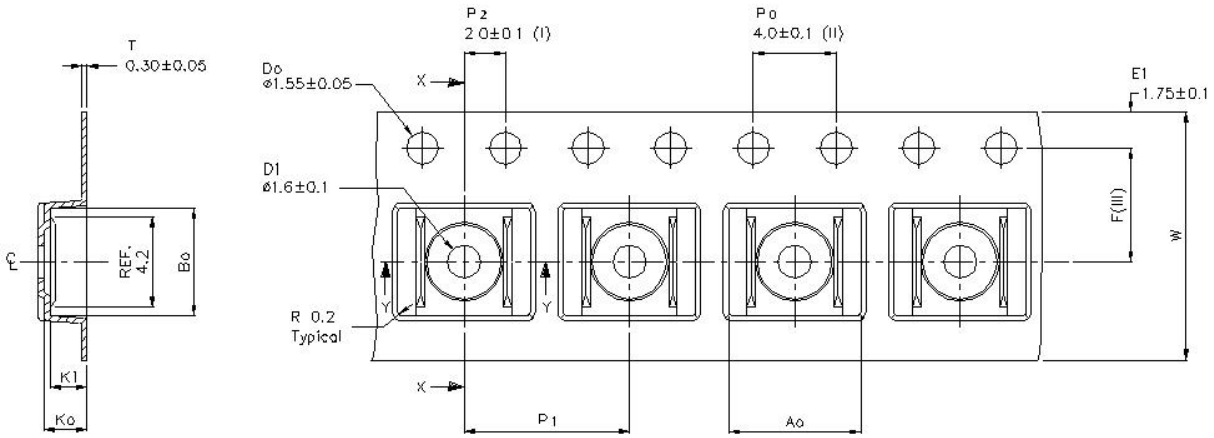
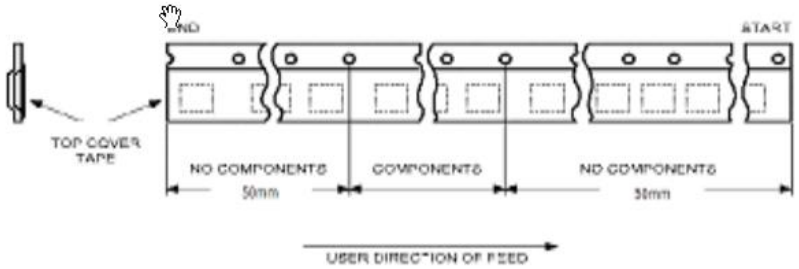


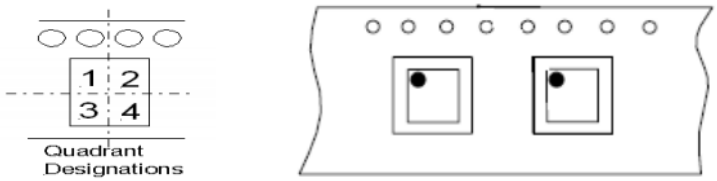
Figure 11.1 Tape/reel digram for SSOP16

Part No.	Package type	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)	F (mm)	P1 (mm)	W (mm)
NSC9260X-QSSR	SSOP16	6.5±0.1	5.3±0.1	2.2±0.1	1.9±0.1	5.5±0.1	8.0±0.1	12.0±0.3

There is no component at the head and the tail of each tape/reel, where the space is 50cm, as shown in the following figure,



Pin 1 is located at the first quadrant，as shown in the following figure,



12. Revision History

Revision	*Description*	*Date*
1.0	Initial Version.	2020/2/13
1.1	Modify some parameters and fonts	2020/06/06
1.2	Revised for uniform formatting and fix some typo.	2021/07/13
1.3	Revised for uniform formatting	2023/07/28

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