NOVOSENSE
纳芯微电子

NSI1042-Q1

Isolated CAN Transceiver

Datasheet (EN) 1.0

Product Overview

The NSI1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1042 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSI1042 is up to 5Mbps. The NSI1042 provides thermal protection and transmit data dominant time out function. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage

  VDD1: 2.5V to 5.5V

  VDD2: 4.5V to 5.5V
- Bus fault protection of -58V to +58V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Data rate: up to 5Mbps
- Ideal Passive, High Impedance Bus and Logic Terminals When Unpowered
- High CMTI: 150kV/μs
- Low loop delay: <220ns
- High system level EMC performance:

  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C ~125°C
- AEC-Q100 Qualified for Grade1
- RoHS-compliant packages: SOP8(300mil), SOP16(300mil)

Safety Regulatory Approvals

- UL recognition:
  - SOP8(300mil): 5000Vrms for 1 minute per UL1577
  - SOP16(300mil): 5700Vrms for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	Package	Body Size
NSI1042-Q1SWVR	SOP8(300mil)	5.85mm ×7.50mm
NSI1042-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

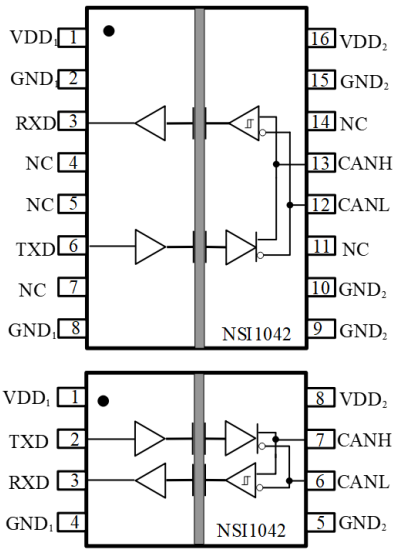

Figure 1. NSI1042 Block Diagram

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1. Pin Configuration and Functions

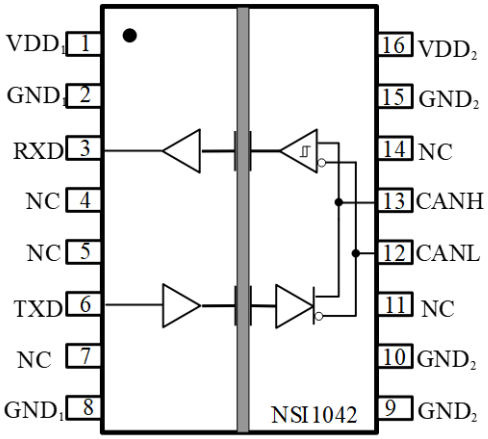


Figure 1.1 NSI1042-Q1SWR SOP16(300mil) Package

Table 1.1 NSI1042-Q1SWR SOP16(300mil) Pin Configuration and Description

NSI1042-Q1SWR PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	NC	No Connection
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Bus Side
10	GND_2	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND_2	Ground 2, the ground reference for Isolator Bus Side
16	VDD_2	Power supply for Bus Side

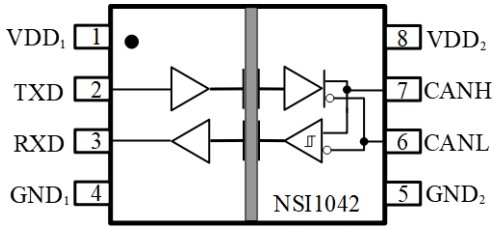


Figure 1.2 NSI1042-Q1SWVR SOP8(300mil) Package

Table 1.2 NSI1042-Q1SWVR SOP8(300mil) Pin Configuration and Description

NSI1042-Q1SWVR PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD_1, VDD_2	-0.5		6.5	V	
Maximum Input Voltage	V_{TXD}	-0.4		VDD_1+0.4	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-58		+58	V	
Output current	I_o	-15		15	mA	
Operating Temperature	T_{opr}	-40		125	°C	
Storage Temperature	T_{stg}	-65		150	°C	

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±6000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, controller side	V_{CC1}	2.5		5.5	V	
Supply voltage, bus side	V_{CC2}	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-30		30	V	
High-level input voltage	V_{IH}	2		5.5	V	TXD
Low-level input voltage	V_{IL}	0		0.8	V	TXD
High-level output current	I_{OH}	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I_{OL}			70	mA	Driver
				4	mA	Receiver
Ambient Temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	θ_{JA}	100	69.9	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	40.8	31.8	
Junction-to-board thermal resistance	θ_{JB}	51.8	29	

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, T_A= 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDD_1	2.5		5.5	V	
	VDD_2	4.5	5	5.5	V	
Logic side supply current	IDD_1		1.97	3.50	mA	VDD_1=3.3V, TXD=0
			0.97	2.00	mA	VDD_1=3.3V, TXD=VCC1
			2.02	3.50	mA	VDD_1=5V, TXD=0
			1.02	2.00	mA	VDD_1=5V, TXD=VCC1
Bus side supply current	IDD_2		46	70	mA	VI=0V, R_{Load} =60Ω
			5.54	10	mA	VI=VDD_2
Thermal-Shutdown Threshold	T_{TS}	155	165	180	°C	
Common Mode Transient Immunity	CMTI	±100	±150		kV/μs	
Logic Side						
High level input voltage	V_{IH}	2			V	TXD pin
Low level input voltage	V_{IL}			0.8	V	TXD pin
High level input current	I_{IH}			10	μA	TXD pin
Low level input current	I_{IL}	-10			μA	TXD pin
Output Voltage High	V_{OH}	VDD_1-0.4			V	I_{OH} = -4mA, RXD pin
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA, RXD pin
Input Capacitance	C_{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.48	4.5	V	TXD=0V, R_{Load} =60Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.25	2.25	V	TXD=0V, R_{Load} =60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0.5*VDD2	3	V	TXD=VDD1, R_{Load} =60Ω
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	VCC=5V, TXD=0, R_{Load} =60Ω, see Figure 6.1
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.05		0.05	V	VCC=5V, TXD=VIO, R_{Load} =60Ω, see Figure 6.1

Parameters	Symbol	Min	Typ	Max	Unit	Comments
		-0.1		0.1	V	VCC=5V, TXD=V_{IO}, NO Load, see Figure 6.1
Dominant short-circuit output current	$I_{O(sc)dom}$	-100		-40	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANH}=-30V
		40		100	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANL}=30V
Recessive short-circuit output current	$I_{O(sc)rec}$	-5		5	mA	Normal mode; V_{TXD} = VDD1, V_{CANH} = V_{CANL} = -27 V to +30 V
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	-12V<V_{COM}<+12V
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	
Hysteresis voltage	V_{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	-5		5	µA	V_{CANH} /V_{CANL} = 5V, VCC = 0V, V_{IO}= 0V
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	19	33	52	kΩ	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V, R_{ID}=R_{CANH}+R_{CANL}
Input resistance	R_{IN}	9	16	28	kΩ	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V
Input resistance matching	RI_{match}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-30		+30	V	

6.2. Switching Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{loop1}		90	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 6.6
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 6.6
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns
		155		210	ns	$t_{bit(TXD)}$ = 200 ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns
		120		220	ns	$t_{bit(TXD)}$ = 200 ns
Driver						
Propagation delay time, recessive -to- dominant output	t_{PLH}		52		ns	see Figure 6.3
Propagation delay time, dominant -to- recessive output	t_{PHL}		73		ns	see Figure 6.3
Differential output signal rise time	t_r		64		ns	see Figure 6.3
Differential output signal fall time	t_f		52		ns	see Figure 6.3
Bus dominant time-out time	t_{TXD_DTO}	800	2000	4000	µs	see Figure 6.7
Receiver						
Propagation delay time, low-to-high-level output	t_{PLH}		32		ns	see Figure 6.5
Propagation delay time, high-to-low-level output	t_{PHL}		35		ns	see Figure 6.5
RXD signal rise time	t_r		3		ns	see Figure 6.5
RXD signal fall time	t_f		3		ns	see Figure 6.5

6.3. Parameter Measurement Information

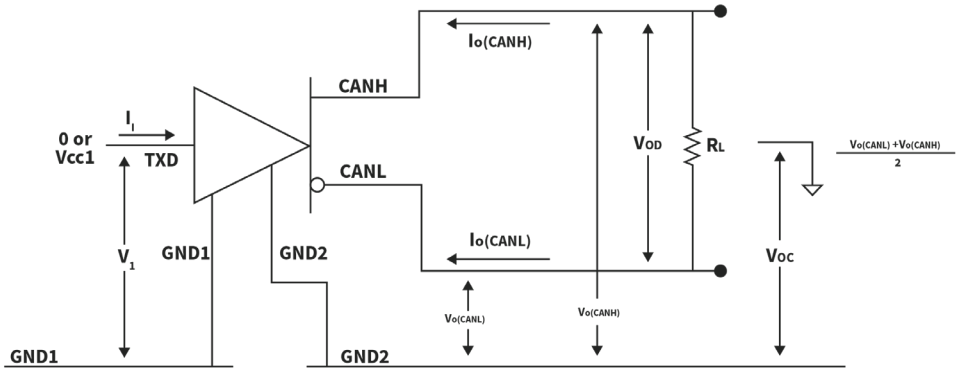


Figure 6.1. Driver Voltage, Current and Test Definitions

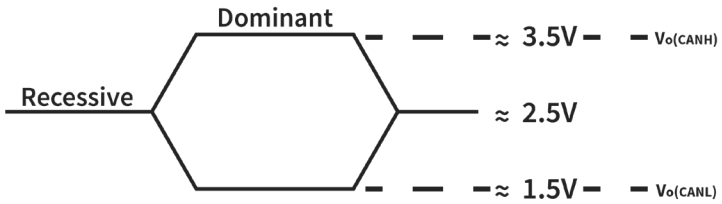
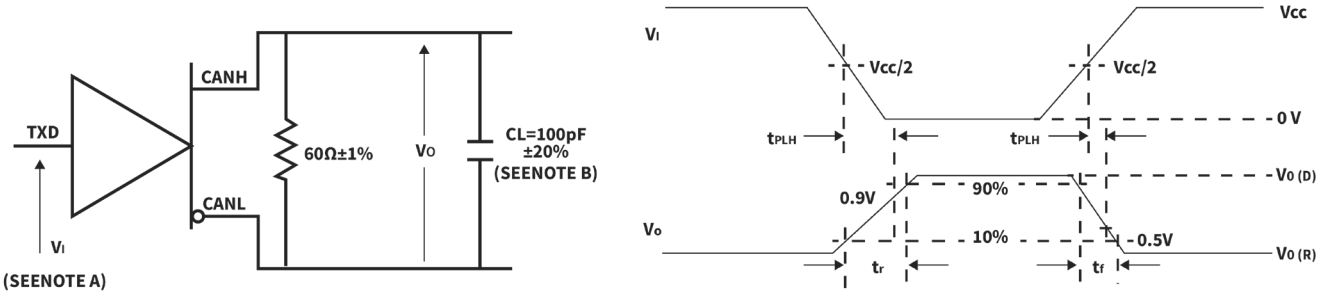


Figure 6.2. Bus Logic State Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 6.3. Driver Test Circuit and Voltage Waveform

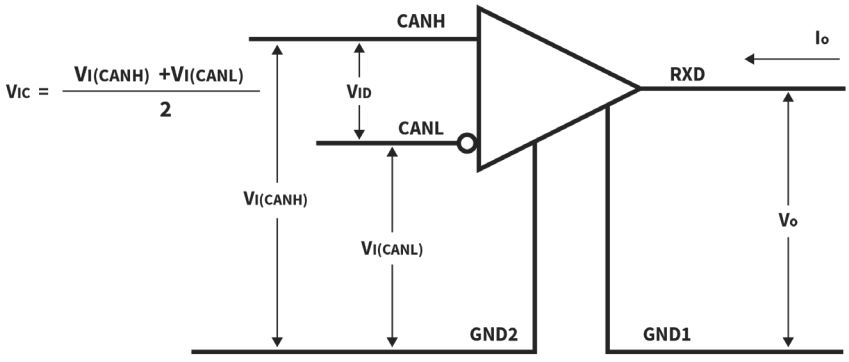
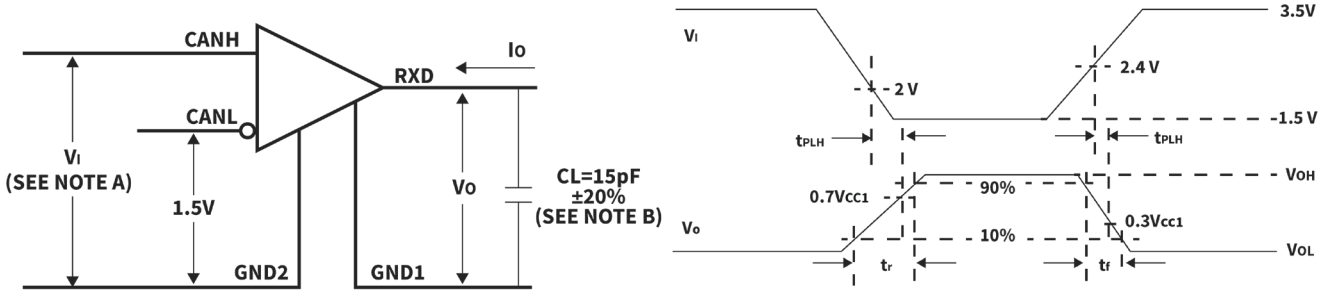


Figure 6.4. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6.5. Receiver Test Circuit and Voltage Waveform

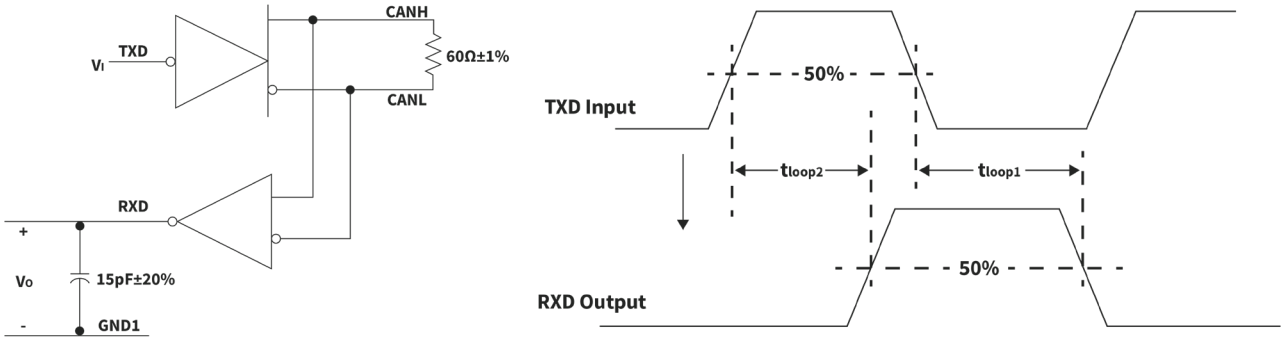
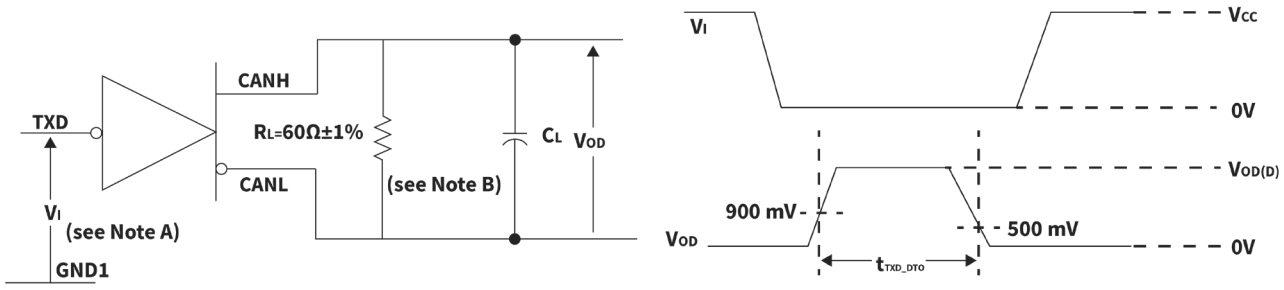


Figure 6.6. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6.7. Dominant Time-out Test Circuit and Voltage Waveform

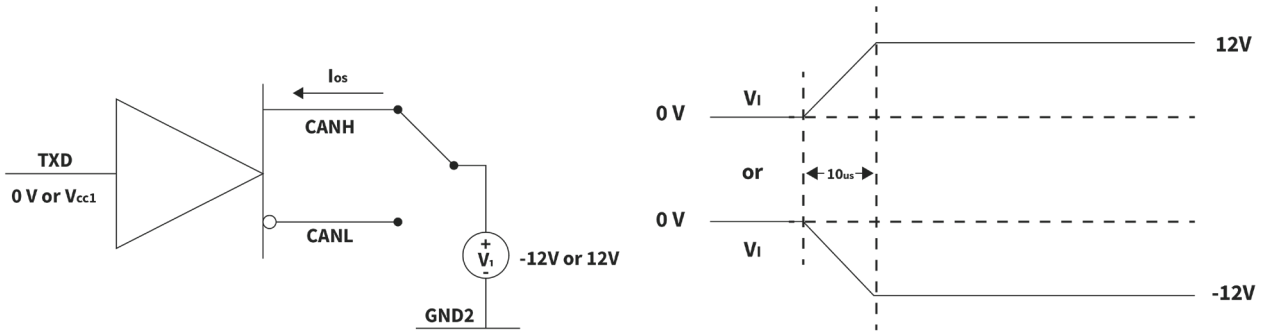


Figure 6.8. Driver Short-Circuit Current Test Circuit and Waveform

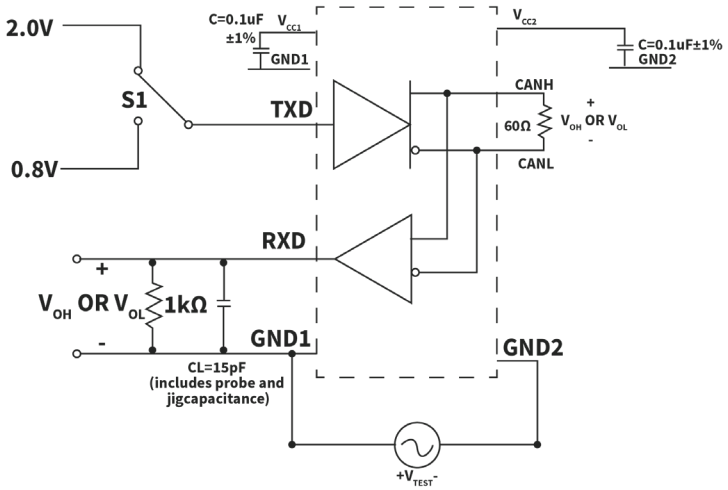


Figure 6.9. Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Description	Symbol	Value		Unit	Comments
		SOP8(300mil)	SOP16(300mil)		
Minimum External Clearance	CLR	8	8	mm	
Minimum External Creepage	CPG	8	8	mm	
Distance Through Insulation	DTI	28		μm	
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	
Material Group		I			

Description	Test Condition	Value	
		SOP8(300mil)	SOP16(300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III	I to III
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8(300mil)	SOP16(300mil)	
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC voltage		2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.6*V_{IORM}$, t_m=10s				
	Method b, routine test (100%				

	production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)				
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥ V_{IMP} × 1.3	V_{IOSM}	10000	10000	V_{PEAK}
Isolation Resistance	V_{IO} =500V, T_A =25°C	R_{IO}	>10^{12}		Ω
	V_{IO} =500V, 100°C ≤ T_A ≤ 125°C		>10^{11}		
	V_{IO} =500V, T_A =T_s		>10^{9}		
Isolation Capacitance	f = 1MHz	C_{IO}	1.2		pF
Insulation Specification per UL1577					
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification) V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, (100% production test)	V_{ISO}	5000	5700	V_{rms}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1042-Q1SWVR

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{θJA}$ = 100 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1250	mW
Safety Supply Current	$R_{θJA}$ = 100 °C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	250	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOP8(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

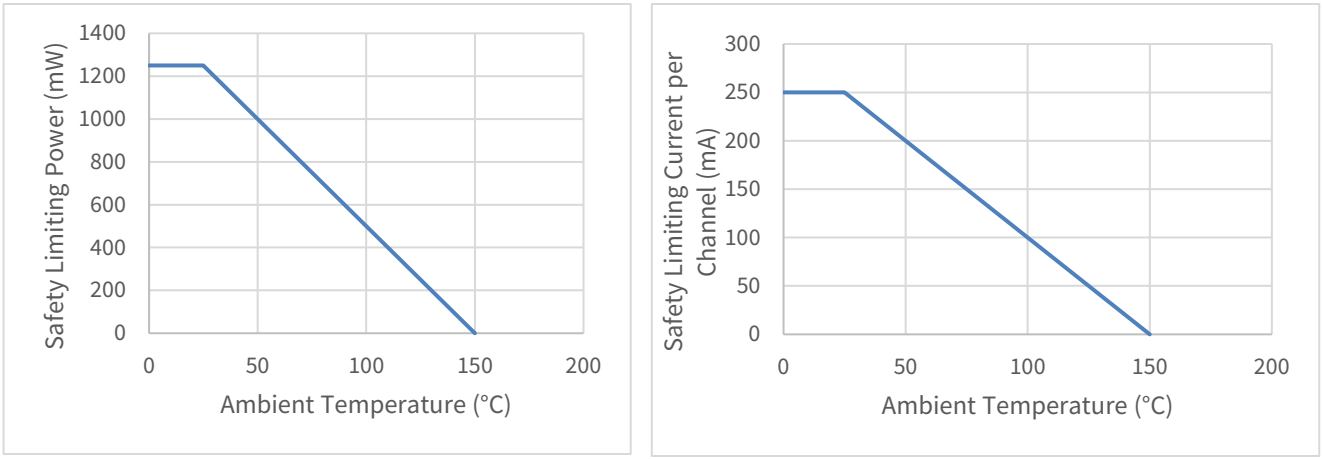


Figure 7.1 NSI1042-Q1SWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1042-Q1SWR

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 69.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1788	mW
Safety Supply Current	$R_{\theta JA}$ = 69.9 °C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	357	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

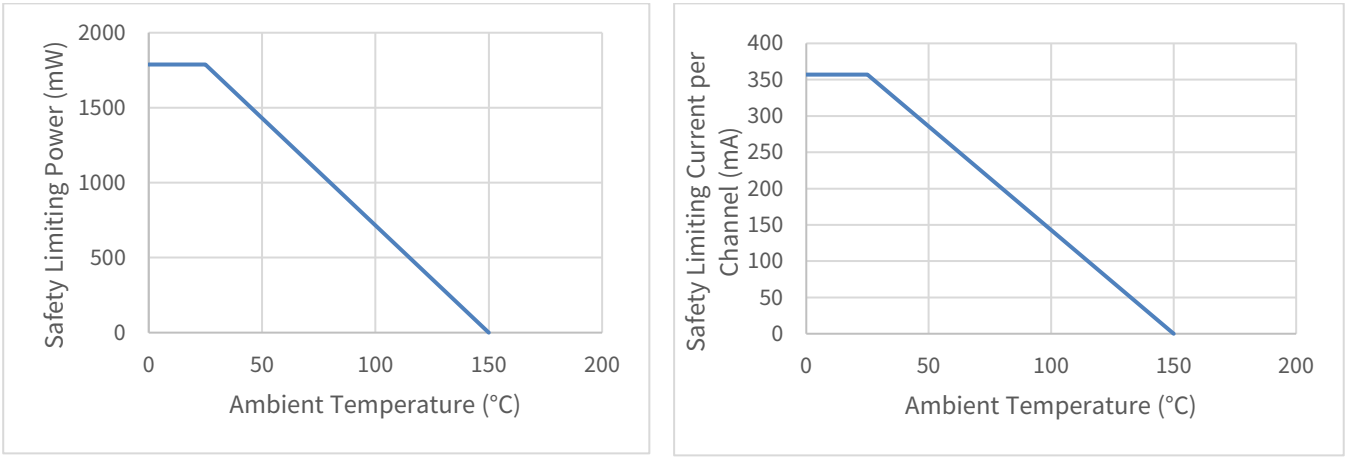


Figure 7.2 NSI1042-Q1SWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

7.4. Regulatory information

The NSI1042-Q1SWR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation
File (pending)	File (pending)	File (pending)	File (pending)

The NSI1042-Q1SWVR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation
File (pending)	File (pending)	File (pending)	File (pending)

8. Function Description

The NSI1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1042 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSI1042 is up to 5Mbps. The NSI1042 provides thermal protection and transmit data dominant time out function.

8.1. Device Functional Modes

Table 8.1. Driver Function Table

TXD	*CANH*	*CANL*	*BUS STATE*
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{CC}/2$

Table 8.2. Receiver Function Table

V_{ID}=CANH-CANL	*RXD*	*BUS STATE*
$V_{ID} \geq 0.9V$	L	Dominant
$0.5V < V_{ID} < 0.9V$	X	Uncertain
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

8.2. TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

8.3. Bus dominant time-out function

In Standby mode, a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is forced HIGH. This prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

8.4. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

8.5. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

9. Application Note

9.1. Typical Application

The NSI1042 requires a 0.1 μF bypass capacitors between VDD1 and GND1, VDD2and GND2. The capacitor should be placed as close as possible to the package. The figure8.1 is the basic schematic of NSI1042.

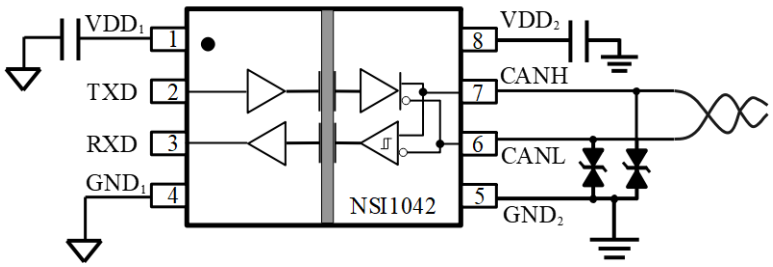


Figure 9.1 Basic schematic of NSI1042

9.2. PCB Layout

The recommended PCB layout shown below.

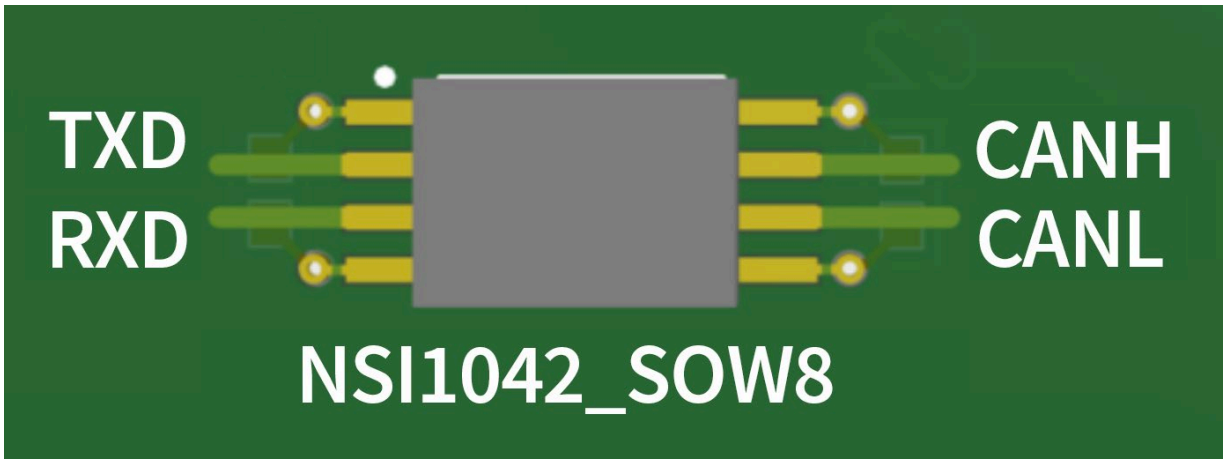


Figure 9.2 Recommended PCB Layout — Top Layer

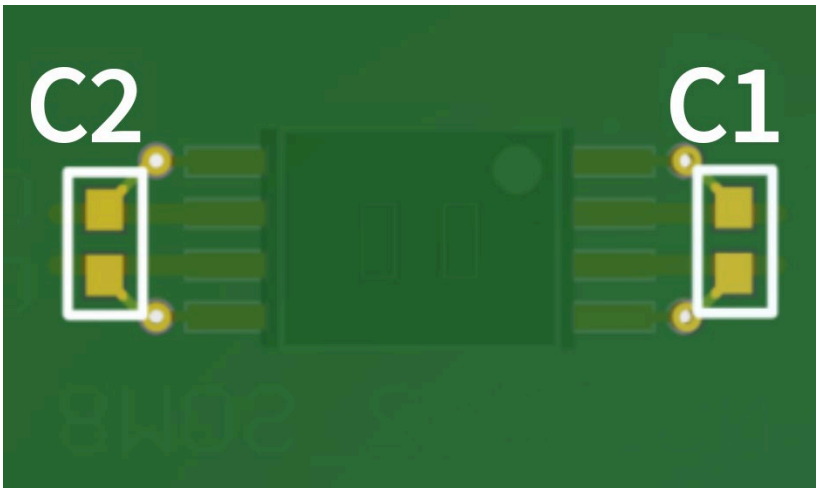
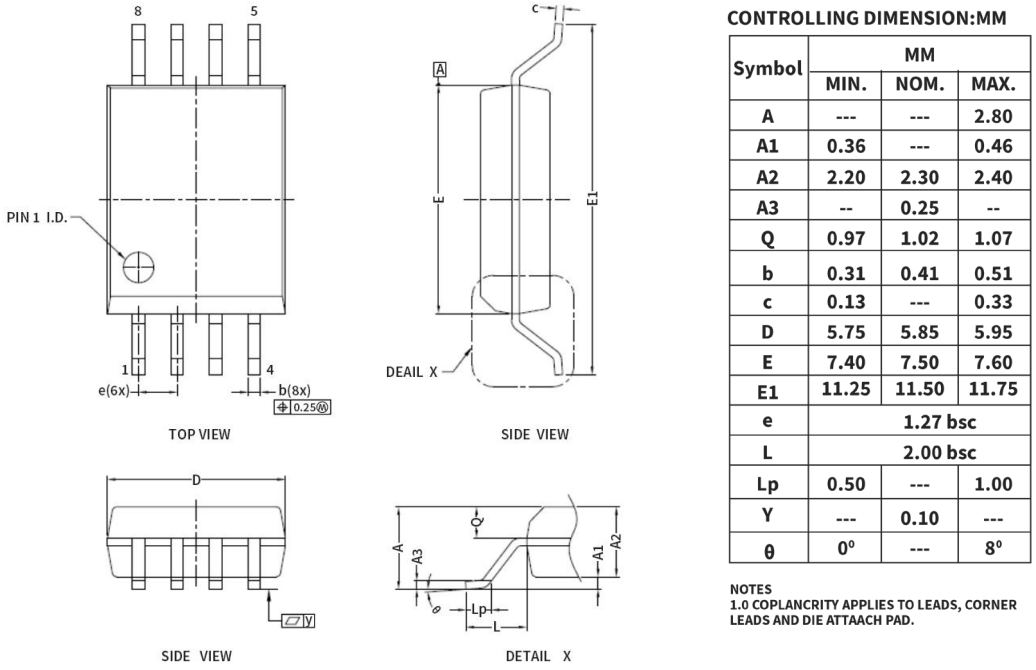


Figure 9.3 Recommended PCB Layout — Bottom Layer

10. Package Information



Symbol	MM		
	MIN.	NOM.	MAX.
A	---	---	2.80
A1	0.36	---	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	---	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	---	1.00
Y	---	0.10	---
θ	0°	---	8°

NOTES
1.0 COPLANCRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTAACH PAD.

Figure 10.1 SOP8(300mil) Package Shape and Dimension in millimeters

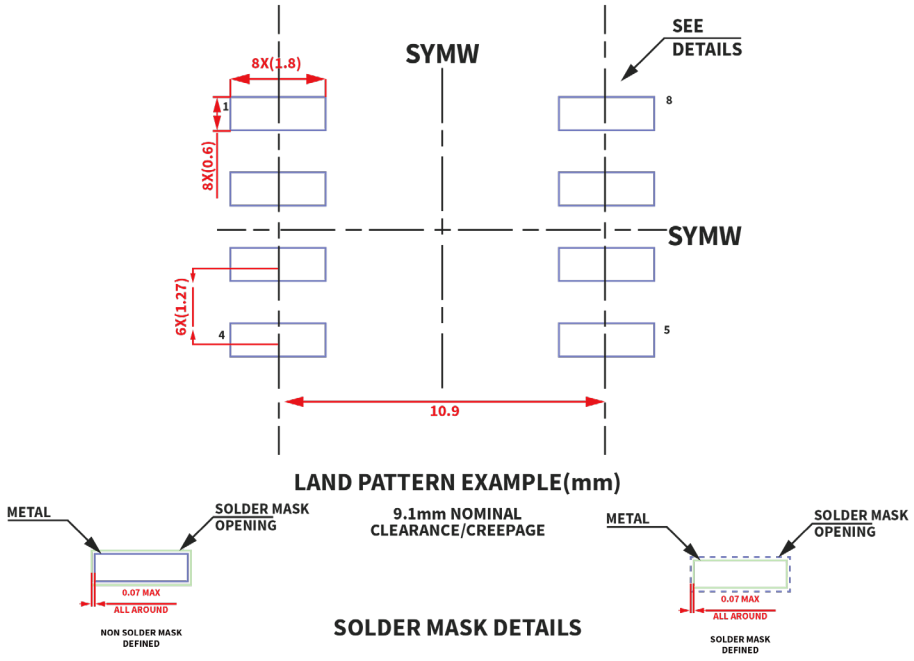
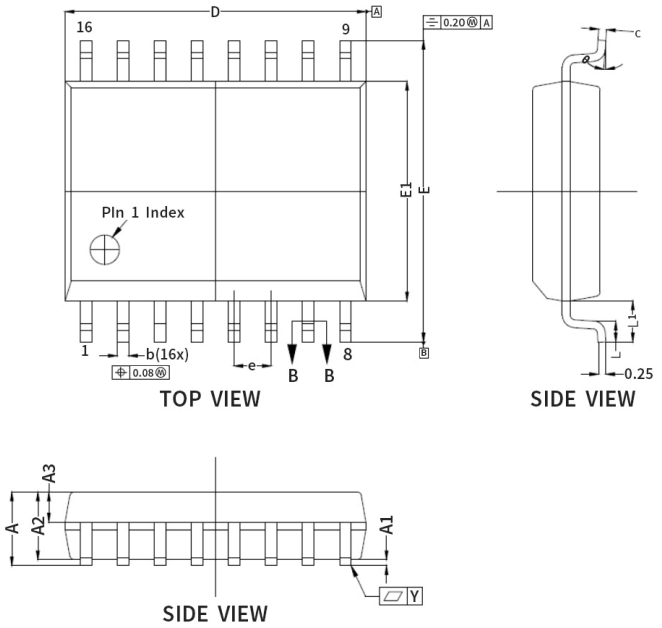


Figure10.2 SOP8(300mil) Package Board Layout Example



CONTROLLING DIMENSION:MM

Symbol	MM		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.11	---	0.30
A2	2.25	2.30	2.35
A3	--	0.25	--
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	2.00 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 10.3 SOP16(300mil) Package Shape and Dimension in millimeters

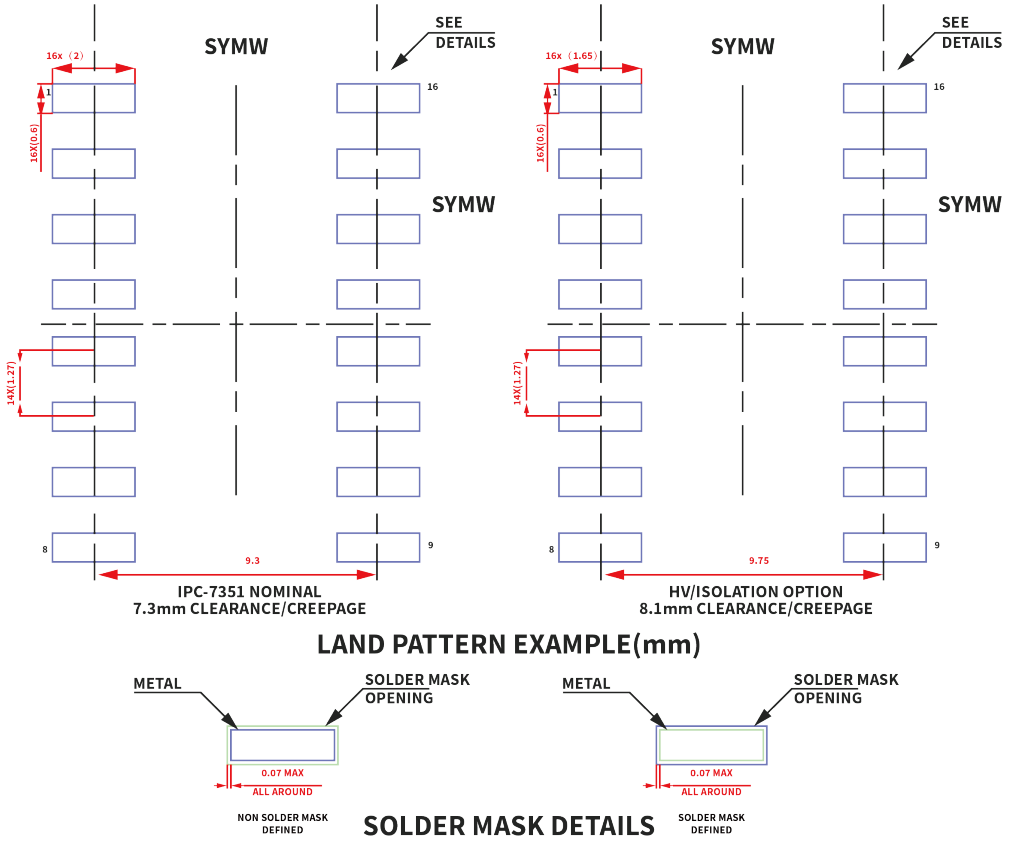


Figure 10.4 SOP16(300mil) Package Board Layout Example

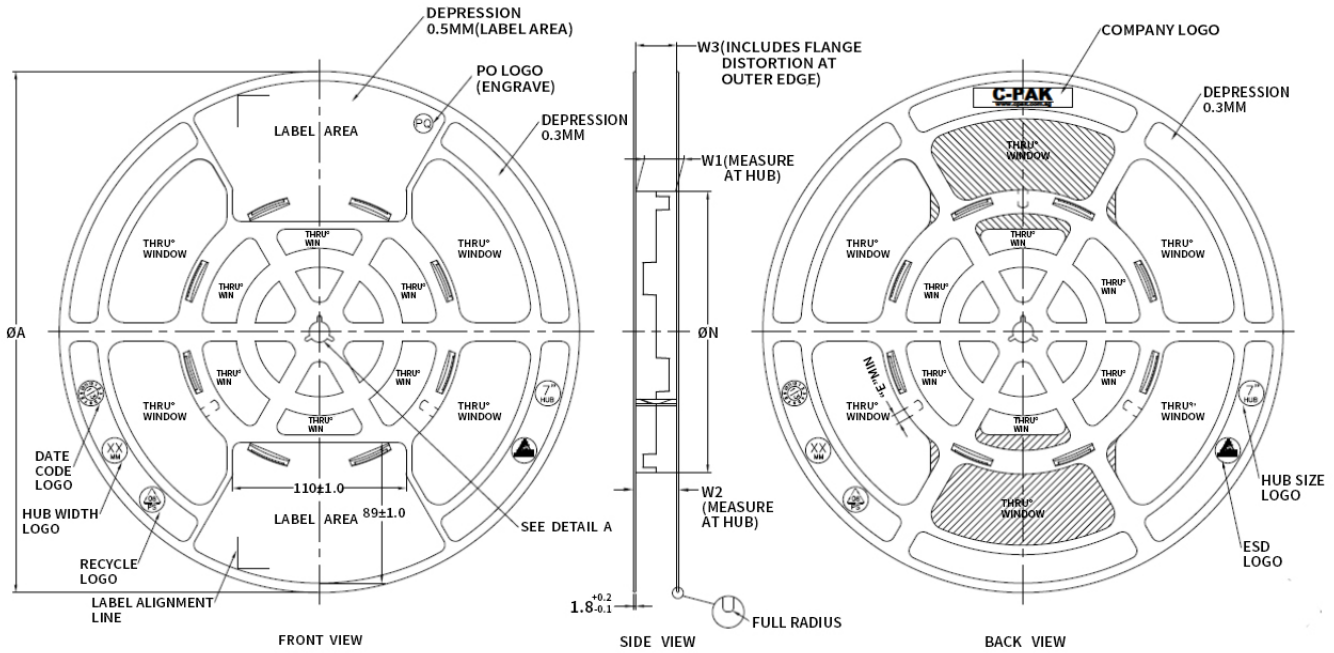
11. Order Information

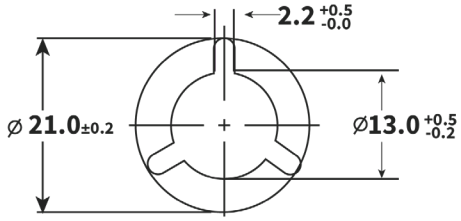
Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI1042-Q1SWVR	5	5 (CAN FD)	-40 to 125°C	3	SOP8 (300mil)	SOW8	1000
NSI1042-Q1SWR	5.7	5 (CAN FD)	-40 to 125°C	2	SOP16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. All devices are AEC-Q100 (Grade 1) qualified.							

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1042	Click here	Click here	Click here	Click here

13. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)

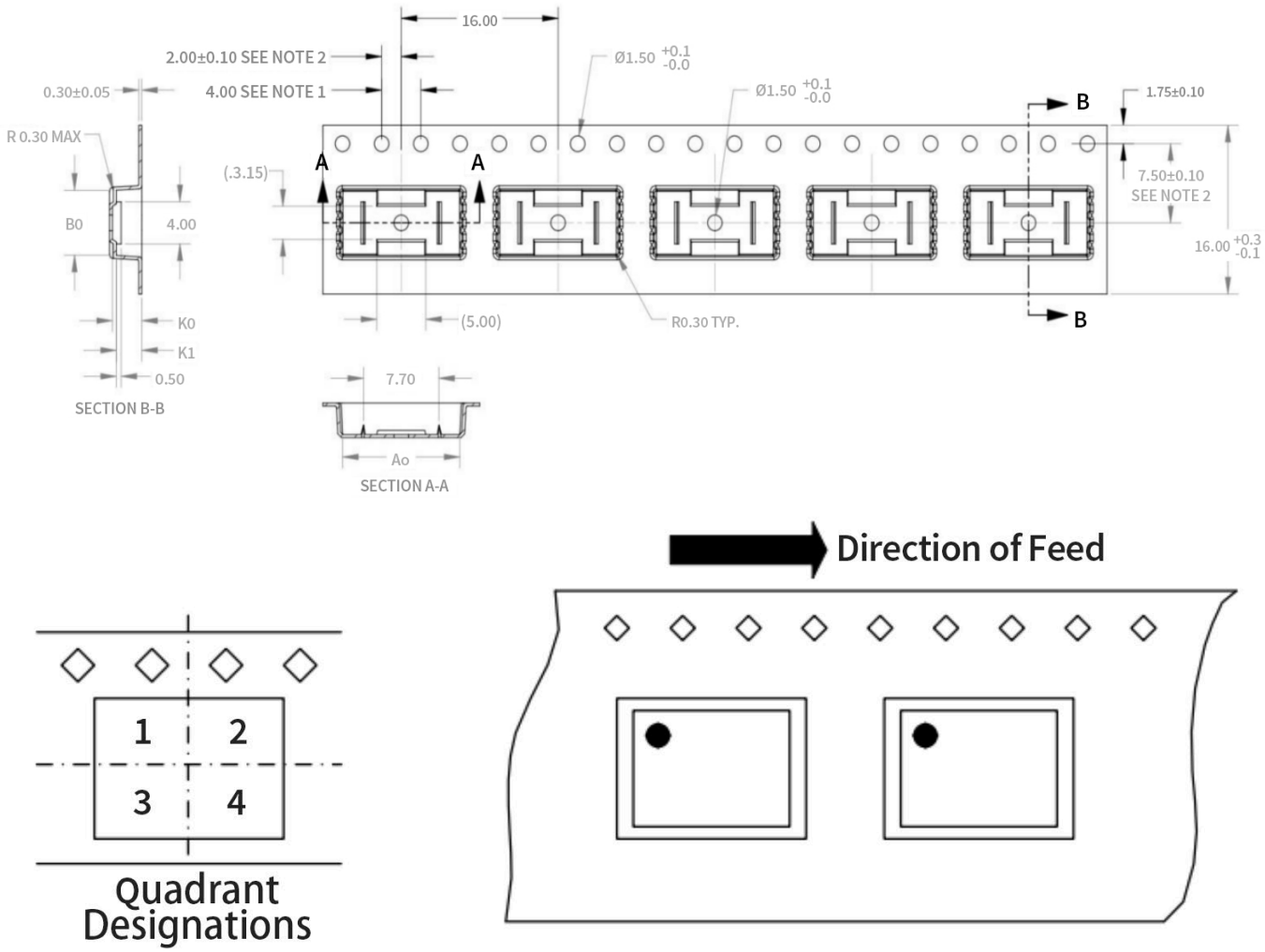
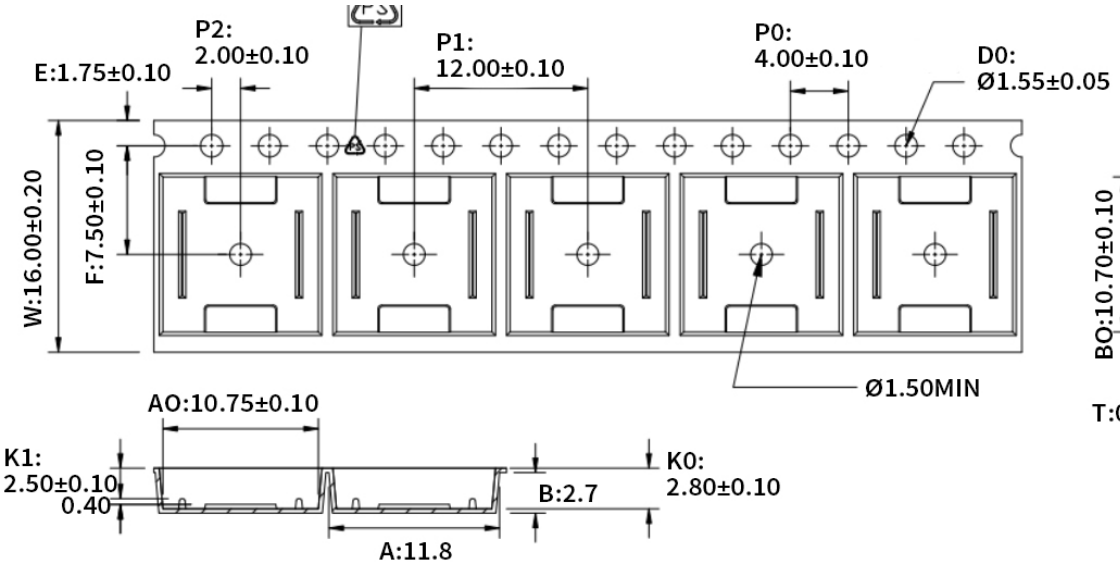


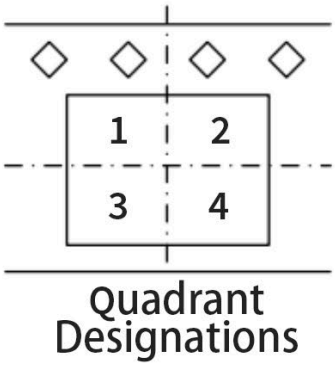
Figure 13.2 Tape Information of SOW8



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(復卷 N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ 10^{10}Ω/口

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



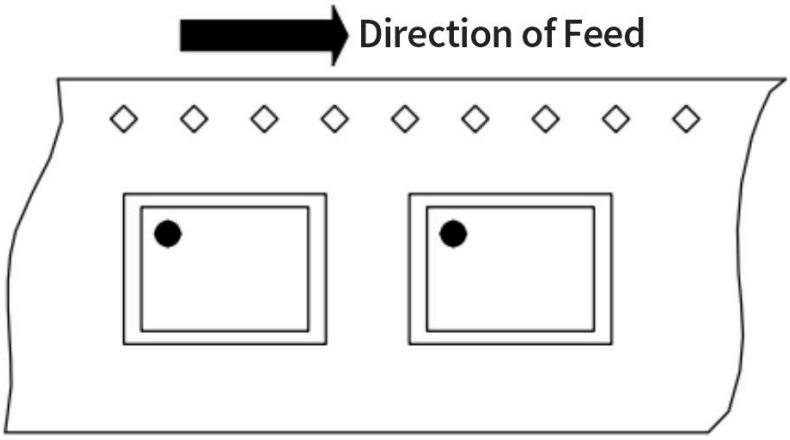


Figure 13.3 Tape and Reel Information of SOW16

14. Revision History

Revision	Description	Date
1.0	Initial version	2023/12/15

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