NSR10A01

100V, 500mA, High Efficiency, Asynchronous Step-down DC-DC Converter

Datasheet (EN) 1.0

Product Overview

The NSR10A01 is an asynchronous step-down DC-DC converter with wide input voltage ranging from 9 V to 100 V which designed for a variety of step-down applications. This high voltage converter has an integrated 100 V, 500 mΩ N-channel buck switch. The device is easy to implement and is provided in 8 pin MSOP8 package.

The NSR10A01 has an inherent adaptive constant-on-time control with no control loop compensation required. The on-time is set by an external resistor and inversely proportional to V_{IN} when switching.

The NSR10A01 has a cycle-by-cycle 725 mA peak switching current limit with adjustable off-time when current limit.

The NSR10A01 operates in ambient temperatures from –40 °C to 125 °C. The device is available in an 8 pin MSOP8 package.

Key Features

- Wide 9 V to 100 V Input Range
- 725 mA Typical Peak Switching Current Limit
- Integrated 500 mΩ High-Side Power MOSFETs
- Adaptive Constant-on-time Control
- Adjustable On-time Setting
- Precision 2.5 V Feedback Reference Voltage
- Adjustable Current Limit Off-time Setting
- No Control Loop Compensation Required
- Cycle-by-Cycle Current Limit
- Over-Voltage Protection
- Over-Temperature Protection

Applications

- PV Inverter
- E-bike, E-scooter
- Power Tools
- Moto Drives, Inverters
- Drones

Device Information

Part Number	*Package Info*
NSR10A01	3.00 mm × 3.00 mm MSOP8

Typical Application

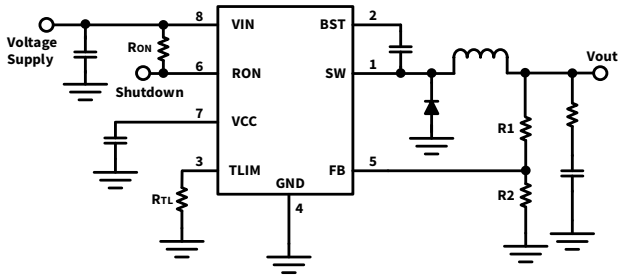

Figure 1 NSR10A01 Typical Application

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1. Pin Configuration and Functions

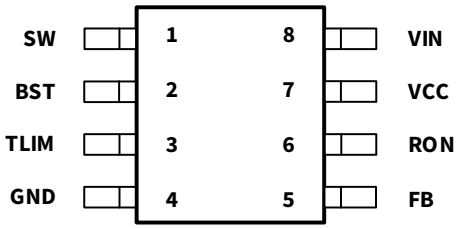


Figure 2 NSR10A01 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	SW	Switching node pin.
2	BST	Boost bootstrap capacitor input. Connect a 10 nF capacitor from BST pin to SW pin.
3	TLIM	Current limit off-time programming pin. A resistor between this pin and GND determines the variation of off-time along with the FB pin voltage per cycle while in current limit.
4	GND	Ground reference.
5	FB	Feedback input pin.
6	RON	On-time set pin. A resistor between this pin and VIN sets the switch on-time as a function of VIN.
7	VCC	7 V output of Internal LDO. It can also be used as a bias input with a >7V external source supply. Do not exceed 14 V.
8	VIN	Power supply pin.

2. Absolute Maximum Ratings

Description	Min	Max	Units
VIN to GND	-0.3	105	V
BST to GND	-0.3	VIN + 6	V
SW to GND	-1	105	V
VCC to GND	-0.3	14	V
TLIM to GND	-0.3	6	V
FB to GND	-0.3	6	V
RON to GND	-0.3	6	V
BST to VCC	-0.3	105	V
BST to SW	-0.3	6	V

3. ESD Ratings

Description	Value	Unit
Electrostatic discharge, Human-body model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	±2000	V
Electrostatic discharge, Charged-device model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (2)	±500	V
Electrostatic discharge, Machine Model (MM)	±200	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. The HBM is a 100-pF capacitor discharge through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin. The machine model ESD compliance level for Pin 5 is 150 V. The human body ESD compliance level for Pin 7 and 8 is 1000 V.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	V_{IN}	9		100	V
Operating Junction Temperature	T_J	-40		125	°C

5. Thermal Information

Parameters(1)	Symbol	MSOP8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	157	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	50	°C/W

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layer board.

6. Specifications

6.1. Electrical Characteristics

(V_{IN}=48V, Ta=-40°C to 125°C. Unless otherwise noted, typical value is at Ta = 25°C.)

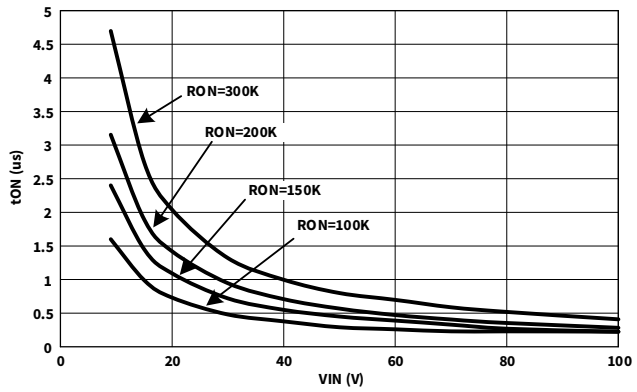
Parameters	Symbol	Min	Typ	Max	Unit	Comments
VIN&VCC						
VCC Regulator Output	V_{CC}	6.6	7	7.4	V	
VCC Current Limit	I_{VCC_CL}		11		mA	
VCC Undervoltage Lockout Voltage	V_{CC_UVLO}		6.3		V	
VCC Undervoltage Hysteresis	$V_{CC\_UVLO\_HYS}$		300		mV	
VCC UVLO Delay (filter)	$t_{VCC\_UV\_DELAY}$		3		µs	
Quiescent Current	I_Q		100	380	µA	Not switching, VFB = 3 V
Shutdown Current	I_{SHD}		6	25	µA	V_{RON} = 0 V
Driver/Power MOSFET/Current limit						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High-side Switch On-State Resistance	$R_{DS(on)\_HS}$		0.52	1.28	Ω	I_{SW}=0.2A, V_{BST}-V_{SW}=5V,
Gate Drive UVLO (VBST-VSW)	V_{GATE_UV}	2.7	3.2	4.9	V	Rising
Gate Drive UVLO Hysteresis	$V_{GATE\_UV\_HYS}$		240		mV	
Breakdown Voltage, VIN to GND	$V_{DS(max)}$	105			V	T_J = 25°C
		101			V	T_J = –40°C to 125°C
Breakdown Voltage, BST to VCC	$V_{BST\_VCC(max)}$	105			V	T_J = 25°C
		101			V	T_J = –40°C to 125°C
Current Limit Threshold	I_{CL}	535	725	900	mA	
Current Limit Response Time	t_{CL_RESP}		225		ns	I_{SW} overdrive = 0.1 A, time to switch off
Minimum Off-time	$t_{OFF(min)}$		300		ns	V_{FB} = 0 V
Off-time	t_{CL_OFF}		17		µs	V_{FB} = 0 V, R_{CL} = 100 kΩ
			2.65		µs	V_{FB} = 2.3 V, R_{CL} = 100 kΩ,
ON-time	t_{ON}	2.15	2.77	3.5	µs	V_{IN} = 10 V, R_{ON} = 200 kΩ,
		290	390	490	ns	V_{IN} = 75 V, R_{ON} = 200 kΩ,
FB/Soft-start/Protection						
FB Reference Threshold	V_{REF}	2.445	2.5	2.550	V	Internal reference
FB Overvoltage Threshold	V_{OV_REF}		2.875		V	Trip point for switch OFF
FB Overvoltage Recovery Threshold	V_{OV_REC}		2.775		V	
FB Bias Current	I_{FB}		100		nA	
RON Shutdown Threshold	V_{SHD}	0.45	0.7	1.1	V	Rising
RON Shutdown Hysteresis	V_{SHD_HYS}		65		mV	
Thermal Shutdown Temperature	T_{SHD}		165		°C	
Thermal Shutdown Hysteresis	T_{HYS}		25		°C	

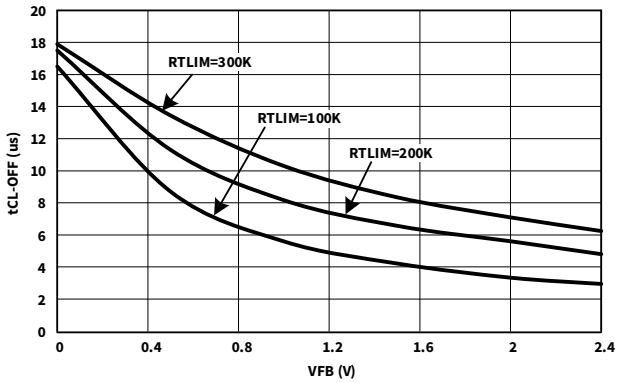
6.2. Typical Characteristics

VIN = 48 V, TA = +25 °C, unless otherwise noted.

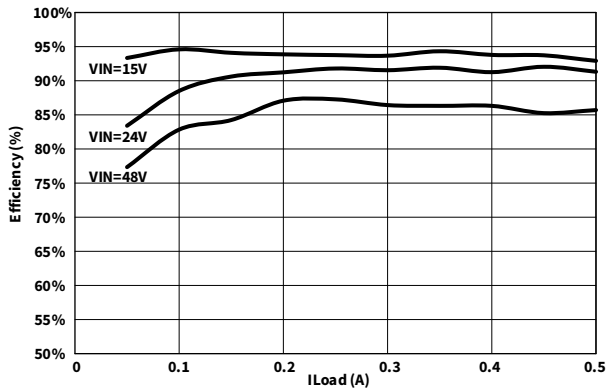
tON vs VIN at different RON



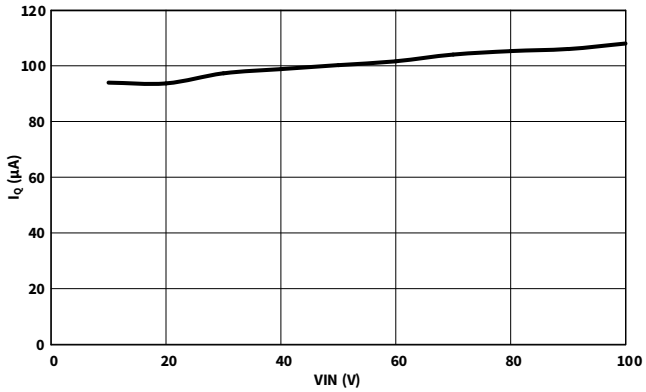
tCL-OFF vs VFB at different RTLIM



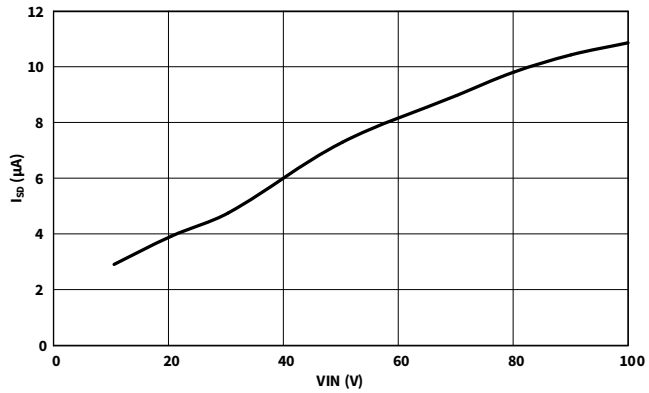
Efficiency curve at 10V output



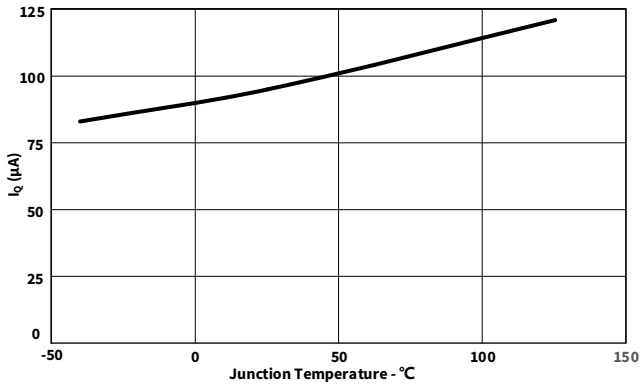
Quiescent Current vs. VIN



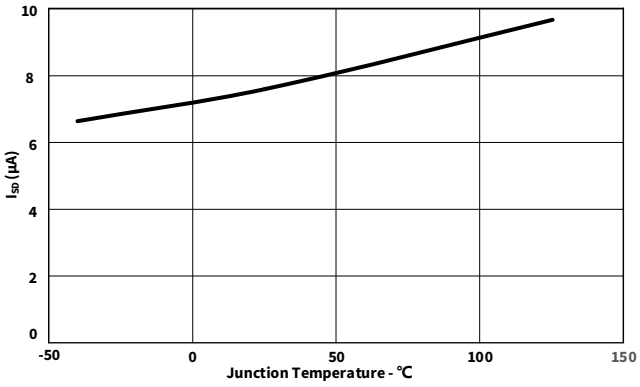
Shutdown Current vs. VIN



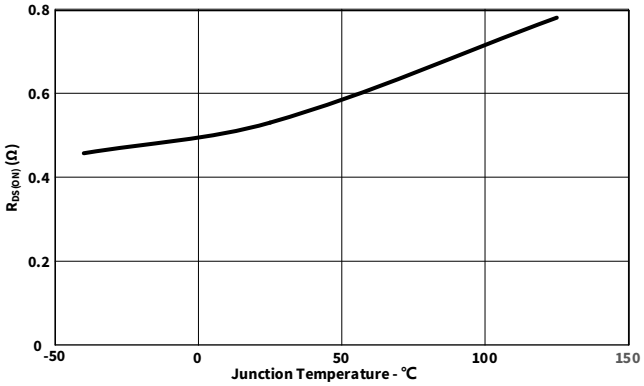
Quiescent Current vs. Junction Temperature



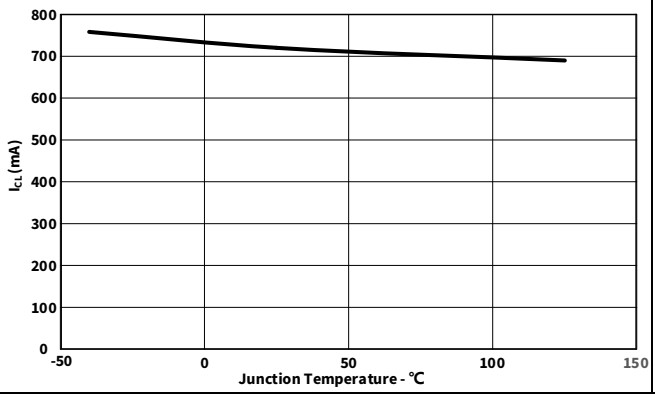
Shutdown Current vs. Junction Temperature



$R_{DS(ON)}$ vs. Junction Temperature



Current Limit vs. Junction Temperature



7. Detailed Description

7.1. Overview

The NSR10A01 is an asynchronous step-down DC-DC converter with wide input voltage ranging from 9 V to 100 V which designed for a variety of step-down applications. This high voltage converter has an integrated 100 V, 500 mΩ N-channel buck switch. The device is easy to implement and is provided in 8 pin MSOP8.

The NSR10A01 has an inherent adaptive constant-on-time control with no control loop compensation required. The on-time is set by an external resistor and inversely proportional to V_{IN} when switching.

The NSR10A01 has a cycle-by-cycle 725 mA peak switching current limit with adjustable off-time when current limit. VCC under-voltage lockout (UVLO), gate drive UVLO and thermal shutdown with automatic recovery are integrated. The pin arrangement is designed for simple and optimized PCB layout with only a few external components.

7.2. Block Diagram

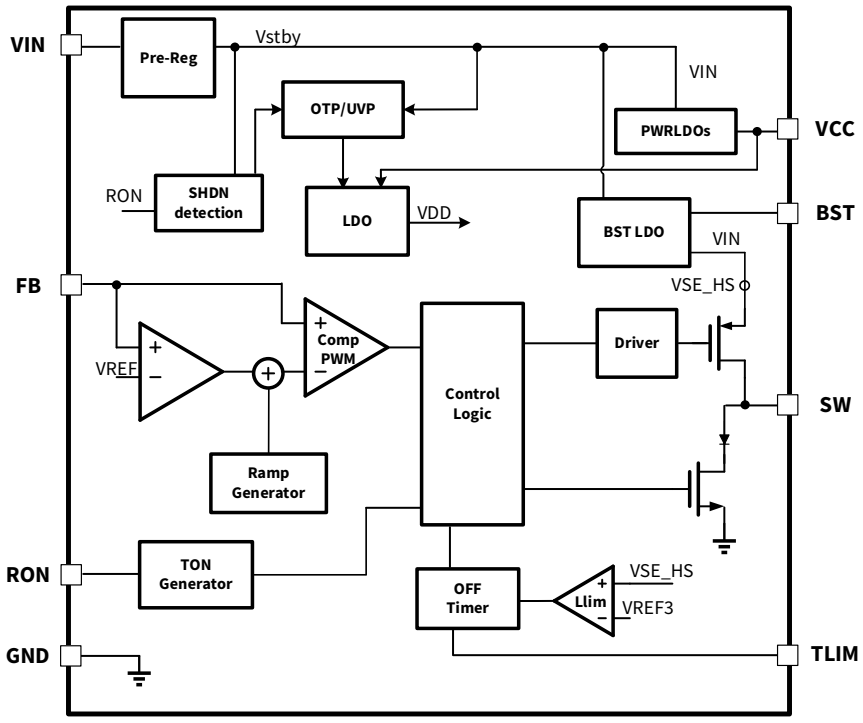


Figure 3 Block Diagram of NSR10A01

7.3. Feature Description

7.3.1 Ton Generator and shutdown

The NSR10A01 adopts COT control mode, has an inherent adaptive constant-on-time control with no control loop compensation required. The on-time is set by an external resistor and inversely proportional to V_{IN} when switching. When the converter works normally, the on-time value is fixed and only related to the values of V_{IN} and R_{ON}, as shown in Equation 1.

$$ton = \frac{1.42\ R_{ON}}{V_{IN}} \cdot 10^{-10} \quad (1)$$

R_{ON} pin also provides a way to turn off the converter. The R_{ON} pin is connected to the V_{IN} pin through resistance, and the converter works normally. When the voltage of the R_{ON} pin is pulled down to less than 0.7 V, the converter will shut down. At this time, the converter will work in a low power consumption state, and the shutdown current is as low as 6 μA. When it is necessary to wake up the converter, remove the pull-down voltage on the R_{ON} pin. By configuring the R_{ON} pin, as shown in the figure 4, the converter can be flexibly enabled and turned off.

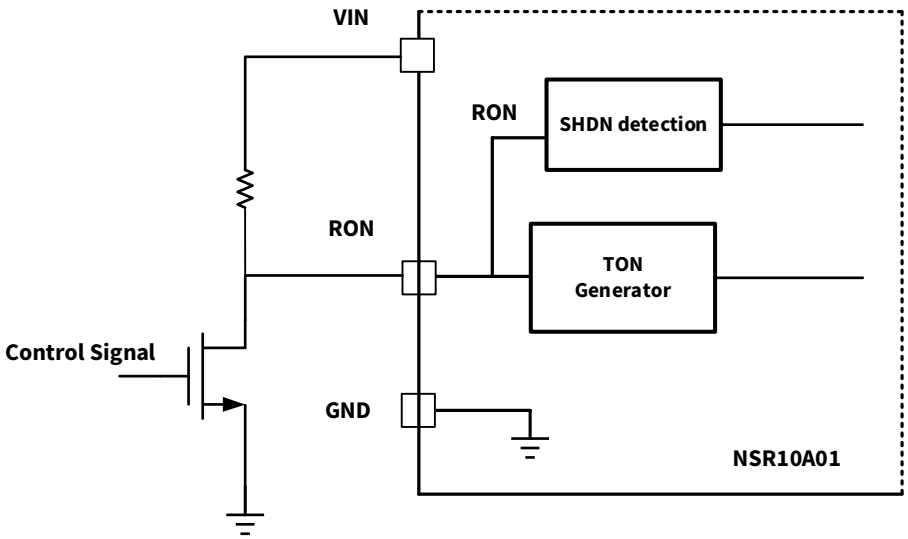


Figure 4 Block Diagram of Shutdown Control

Depending on the load, the converter will work in DCM and CCM modes. When the load is very light, the converter works in DCM mode, the inductor current rises from zero to the peak value during the short on-time, then back to zero during the off-time and remains at zero until the next turn on time interval begins. When the load increases, the operating mode will switch to CCM, which has continuous inductance current and there is no time when the inductance current is zero. According to equation 1 and volt-second balance principle, the operating frequencies of the converter under two operating modes can be obtained.

In DCM mode, the switching frequency is approximately

$$F_{SW\text{-}DCM}= \frac{V_{OUT}^{2}\cdot L}{R_{LOAD}\cdot R_{ON}^{2}}\cdot 10^{20} \quad (2)$$

In CCM mode, the switching frequency is

$$F_{SW\text{-}CCM}= \frac{V_{OUT}}{1.42\cdot R_{ON}}\cdot 10^{10} \quad (3)$$

7.3.2 VCC bias supply

In order to improve the efficiency of the system, if the output voltage is from 7 to 14 V, it can replace the VCC to supply power to the converter, as shown in Figure 5. It is recommended to connect a 100 nF capacitor at the VCC pin.

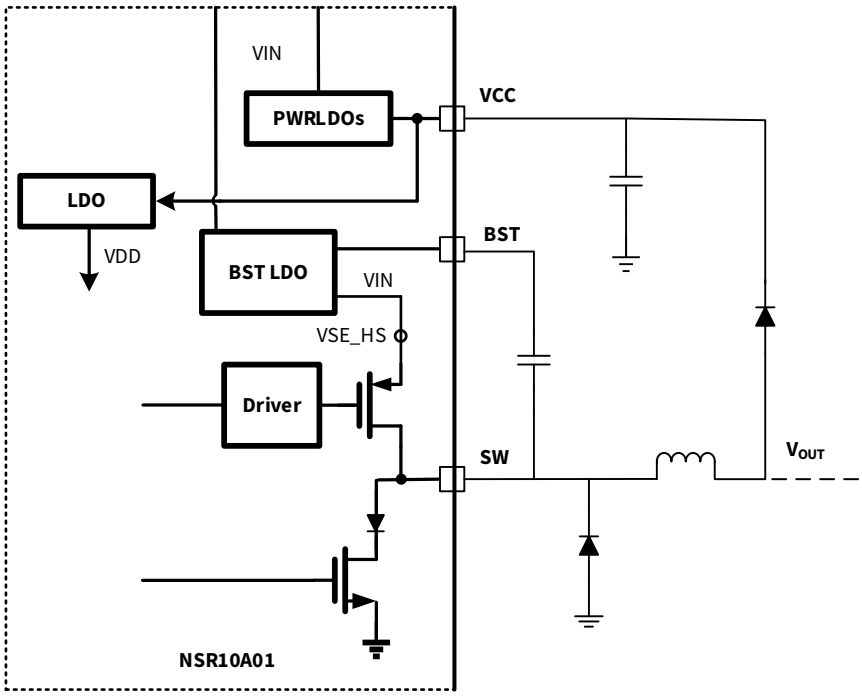


Figure 5 VCC bias supply and Bootstrap capacitor

7.3.3 FB Configuration and Ripple Injection

By configuring the resistance connected to the FB pin, different output voltages can be obtained, as shown in Equation 4.

$$V_{OUT} = 2.5 \cdot (1 + \frac{R_1}{R_2}) \quad (4)$$

The connection relationship between R_1 and R_2 is shown in Figure 1. The feedback comparator depends on the output ripple voltage to switch the working state of the high-voltage N MOS. To make the internal comparator respond to the output voltage quickly, it is recommended to inject 25 mV to 50 mV ripple voltage at the FB pin. A low-cost way is to add additional series resistance at the output capacitor, as shown in Figure 1. To obtain the minimum output voltage ripple, it is recommended to couple the SW waveform to the FB pin through capacitance.

7.3.4 Drive of high-voltage N MOS

The NSR10A01 is internally integrated with high-voltage N MOS, and its gate driver is powered by an external bootstrap capacitor. The bootstrap capacitance is recommended to be 10 nF, which is connected at both ends of BST and SW, as shown in Figure 5. During each cycle when the high-voltage N MOS turns off, the SW voltage is low, the bootstrap capacitor is charged from BST through the internal BST LDO. The converter is designed with minimum off-timer to ensure that there is a minimum interval during every switching cycle to charge the bootstrap capacitor.

7.3.5 Overcurrent Protection and t_{CL-OFF}

The NSR10A01 is internally provided with over-current protection design. When high-voltage N MOS turn on, the converter will detect the inductance current. If the current detected exceeds 725 mA, the converter will turn off the output of the high-voltage N MOS. The off time depends on the FB voltage and R_{TLIM} values, as shown in the equation 5. According to the equation, the current

limit off time is inversely proportional to the FB voltage, the design can balance the protection of the converter when the short circuit occurs and the speed of the converter to resume normal operation when the short circuit disappears.

$$t_{CL\text{-}OFF} = \frac{1}{0.59+\frac{V_{FB}}{7.22\cdot 10^{-6}\cdot R_{TLIM}}} \cdot 10^{-5} \quad (5)$$

It should be noted that the time of current limit response is 225 ns. Therefore, when the short circuit occurs at high V_{IN}, it is necessary to consider whether the circuit can achieve volt-second balance when V_{FB} is 0 and the off time is 17 μs. In order to balance inductor volt-seconds and limit the short-circuit current, it may be necessary to increase the internal resistance of the inductor and the voltage drop of the diode.

7.3.6 Overvoltage Protection

Overvoltage protection design is provided inside the NSR10A01. When FB pin detects that the voltage exceeds 2.875 V, the converter will immediately turn off the output of high-voltage N MOSFET and interrupt the TON Generator. This overvoltage protection design can ensure that the output voltage will not exceed 15 % of the design value.

7.3.7 Thermal Shutdown

The NSR10A01 is internally provided with a thermal shutdown circuit. When junction temperature is detected to exceed 165 °C, the converter will immediately shutdown the output to prevent overheating damage. When the junction temperature is detected to be lower than 140 °C, the converter will start working again.

7.4. Typical Application

7.4.1 Application Circuit

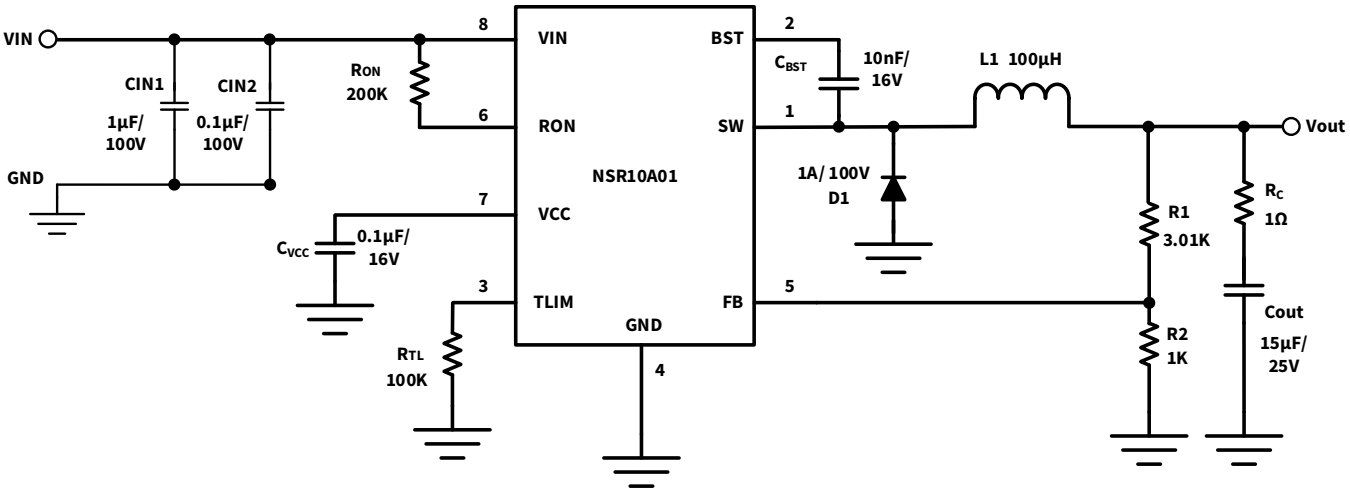
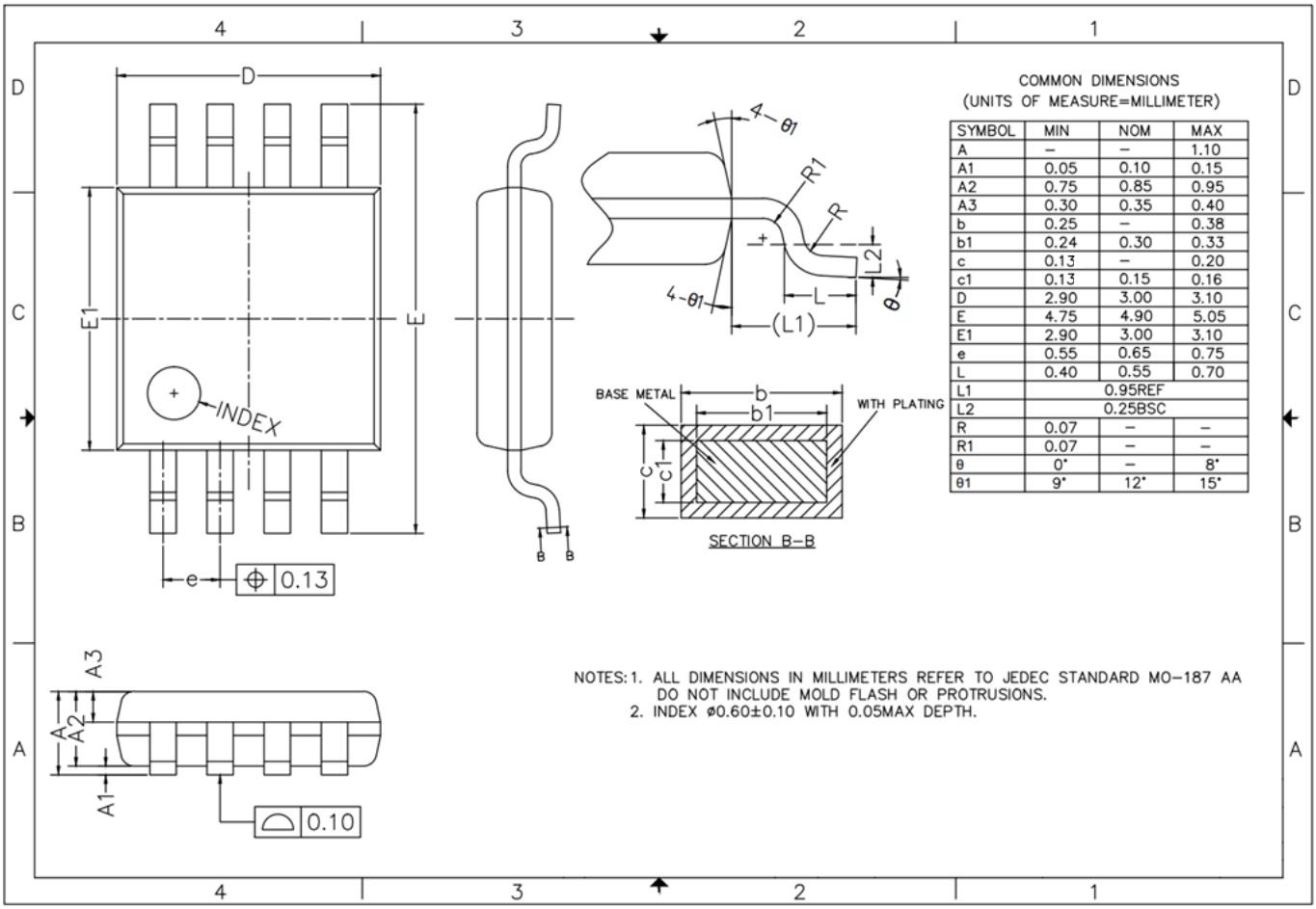


Figure 6 VIN=12 ~ 100 V, VOUT=10 V, IOUT=0 ~ 500 mA

8. Package Information

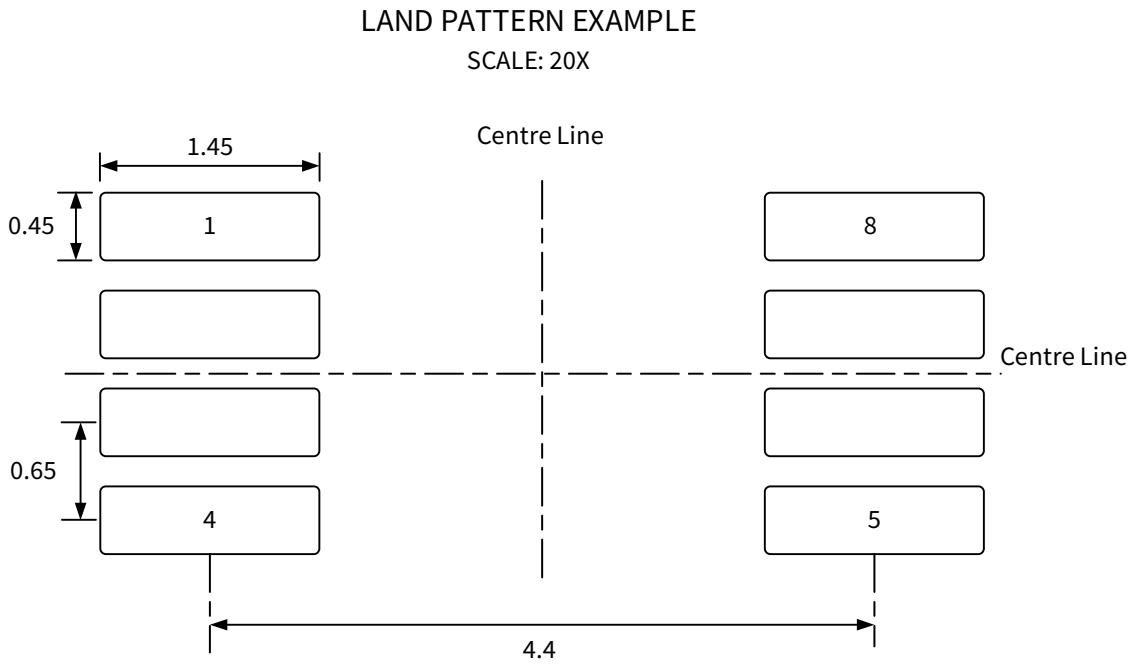
8.1. MSOP8 Package Information

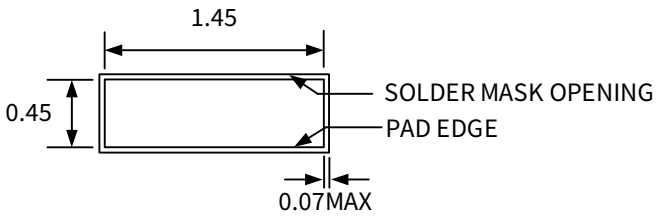


SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.25	–	0.38
b1	0.24	0.30	0.33
c	0.13	–	0.20
c1	0.13	0.15	0.16
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.55	0.65	0.75
L	0.40	0.55	0.70
L1	0.95REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	9°	12°	15°

Figure 7 MSOP8 Package Information

8.2. MSOP8 Recommended Land Pattern



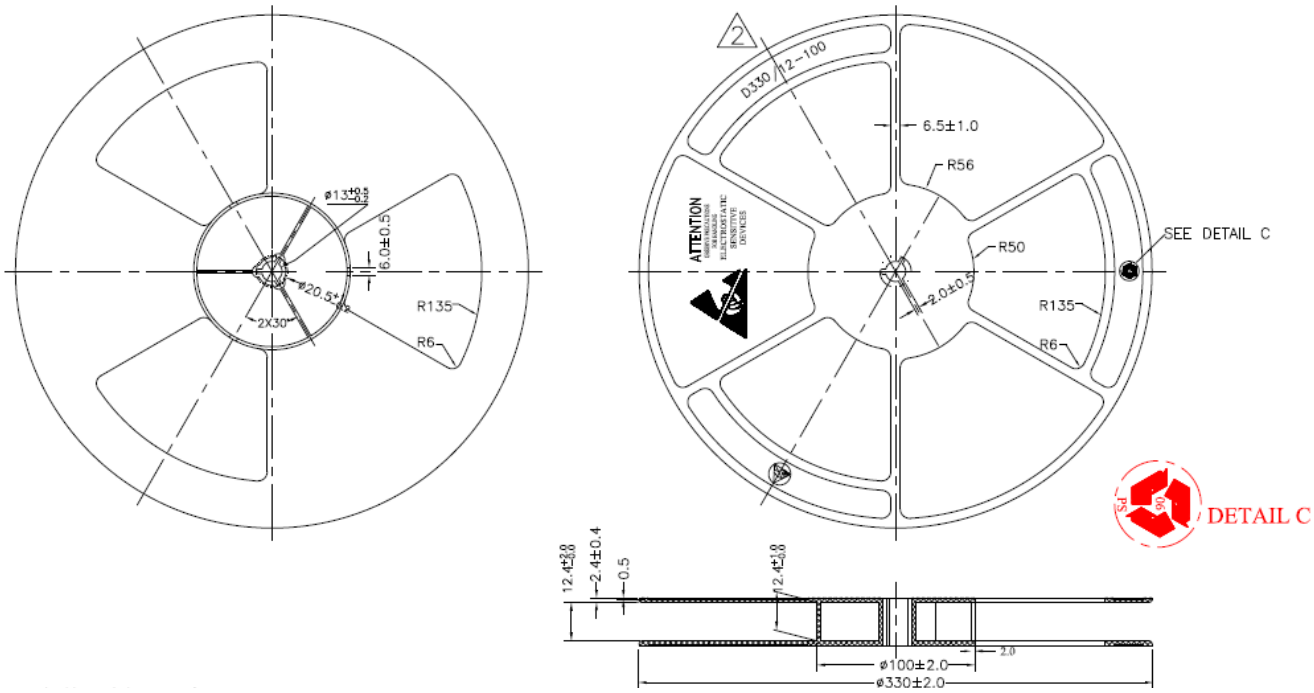


NON-SOLDER MASK
DEFINED PAD

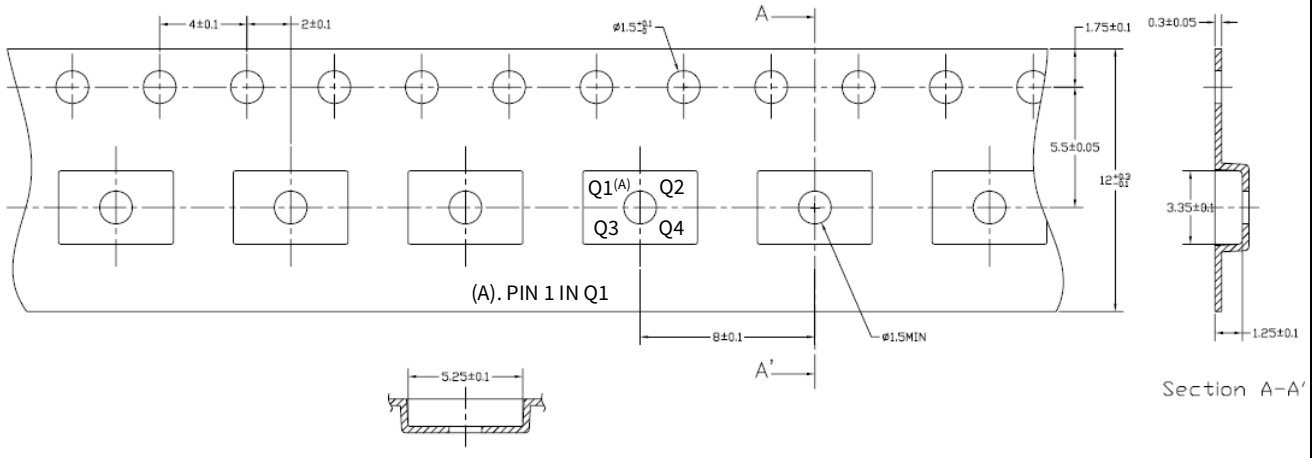
SOLDER MASK DETAILS

NOTES: ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

8.3. Tape and Reel



NOTES:
1. MATERIAL: POLYSTYRENE (BLACK).
2. ALL DIMENSIONS NOTED ARE IN MILLIMETERS.
3. TOLERANCE ON ALL DIMENSIONS (NOT OTHERWISE NOTED) IS ±0.25.



NOTES:
1. MATERIAL:Hard polystyrene(PS)
2. ALL DIMS IN MM
3. There must not be foreign body adhesion and the state of the surface must be excellent
4. The meander of the tape is assumed with 1mm or less every 100mm between 250mm
5. A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.3 up to 50 pitches
6. ø560 Paper-Reel， 60000 pockets(480M)
7. Corner R=0.3max
8. Surface resistance 1X10E5≤ Rss≤1X10E9 0HMS/SQ

9. Order Information

Orderable Part Number	MSL	Package	SPQ	Marking
NSR10A01-DMSR	1	MSOP8	2500	10A01

10. Revision history

Revision	Description	Date
1.0	Initial version	2023/12/8

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