NSI8608

Multi-channel Isolated Digital Input Receiver for Digital Input Modules

Datasheet (EN) 1.0

Product Overview

The NSI8608 is fully-integrated, isolated digital-input receivers with IEC 61131-2 Type 1,2 and 3 characteristics. The device receives 24-V to 60-V digital-input signals and provide isolated digital outputs. Field-side input with no power supply supports sink and source current input through integrated rectifier bridge. The device integrates the current limiting function to effectively reduce the overall temperature of the solution. The voltage transition threshold is compliant with Type 1,2 and 3 and can be increased further using an external resistor.

The NSI8608 uses the "Adaptive OOK" modulation technique to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage.

Key Features

- Up to 3000V_{rms} Insulation voltage
- Date rate: DC to 2Mbps
- Bipolar digital interface with sinking or sourcing inputs
- High Input-Voltage Range: ±60 V
- Compliant to IEC 61131-2 Type 1,2,3
- Accurate Current Limit for Low-Power Dissipation
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 50kV/us
- Chip level ESD: HBM: ±2kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SSOP20

Safety Regulatory Approvals

- UL recognition: up to 3000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Motor Control

Device Information

Part Number	*Package*	*Body Size*
NSI8608-DSSTR	SSOP20	8.65*3.90mm

Functional Block Diagrams

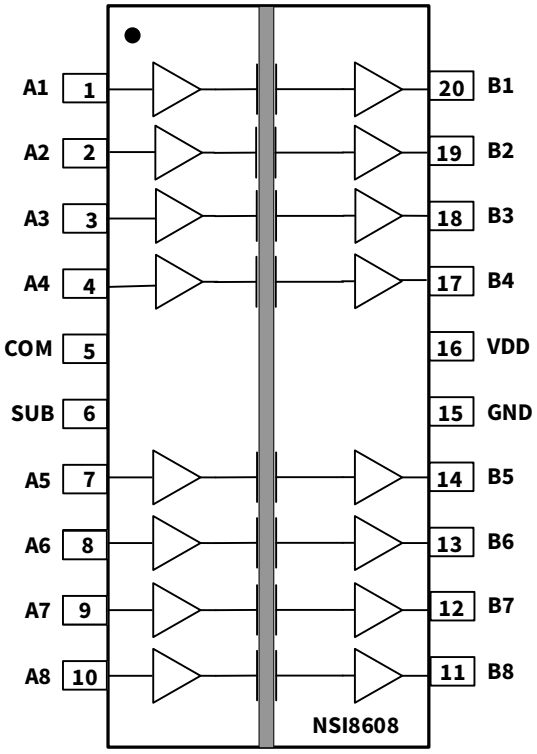

Figure 1. NSI8608 Block Diagram

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1. Pin Configuration and Functions

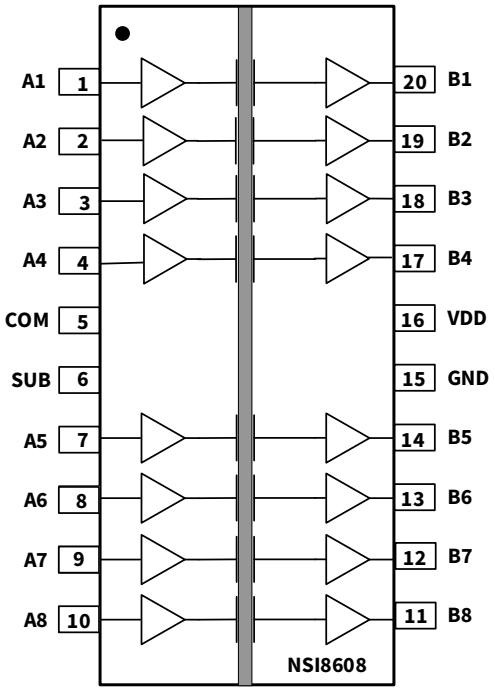


Figure 1.1 NSI8608 Package

Table 1.1 NSI8608 Pin Configuration and Description

NSI8608 PIN NO.	*SYMBOL*	*FUNCTION*
1	A1	Field-side input1
2	A2	Field-side input2
3	A3	Field-side input3
4	A4	Field-side input4
7	A5	Field-side input5
8	A6	Field-side input6
9	A7	Field-side input7
10	A8	Field-side input8
5	COM	Common terminal. Can be connected to ground for sinking inputs or the field supply for sourcing inputs
6	SUB	Internal connection to input chip substrate. This pin must keep floating
20	B1	Channel A1 output
19	B2	Channel A2 output
18	B3	Channel A3 output
17	B4	Channel A4 output
14	B5	Channel A5 output
13	B6	Channel A6 output
12	B7	Channel A7 output
11	B8	Channel A8 output
16	VDD	Power supply, Output side
15	GND	Ground connection for VDD

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, control side	VDD	-0.5		6	V	
Voltage on Bx pins	VBx	-0.5		VDD+0.5	V	
Output current on Bx pins	IO	-15		15	mA	
Voltage on Ax pins	VAx	-60		60	V	
Functional isolation between channels on the field side	V (ISO, FUNC)	-60		60	V	
Junction temperature	Tj	-40		150	°C	
Operating Temperature	Topr	-40		125	°C	
Storage Temperature	Tstg	-65		150	°C	

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD	2.5		5.5	V	
High-level output voltage on Bx	VOH	VDD-0.4			V	IOH = - 4 mA
Low-level output voltage on Bx	VOL			0.4	V	IOL = 4 mA
Data Rate	DR	0		2	Mbps	
Ambient Temperature	Ta	-40		125	°C	

5. Thermal Information

Parameters	Symbol	SSOP20	Unit
Junction-to-ambient thermal resistance	θ_{JA}	67.1	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	21.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	28.2	°C/W

6. Specifications

6.1. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
VDD Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
VDD supply current	IDD		3.15	5	mA	all input low
			3.5	5	mA	all input high
			3.5	5	mA	all input 125kHz
			4	6	mA	all input 1MHz
High-level output voltage on Bx	VOH	VDD-0.4			V	IOH = - 4 mA
Low-level output voltage on Bx	VOL			0.4	V	IOL = 4 mA
current drawn from Ax pin	IAx	1.55	2.1	2.62	mA	VIL≤|VAx|≤60V
High level threshold	VIH		8	9.2	V	voltage at Ax
Low level threshold	VIL	6.1	7.3		V	
Threshold voltage hysteresis	VHYS		0.7		V	
Output signal rise and fall time, Bx pins	tr, tf		3		ns	See Figure 6.3, C_L = 15pF
Propagation delay time for low to high transition	tPLH			380	ns	See Figure 6.3, C_L = 15pF
Propagation delay time for high to low transition	tPHL			150	ns	See Figure 6.3, C_L = 15pF
Pulse skew |tPHL - tPLH|	tsk(p)		150		ns	
Minimum pulse width	tUI	500			ns	
Common mode transient immunity	CMTI	50	75		kV/us	See Figure 6.4, C_L = 15pF

6.2. Typical Performance Characteristics

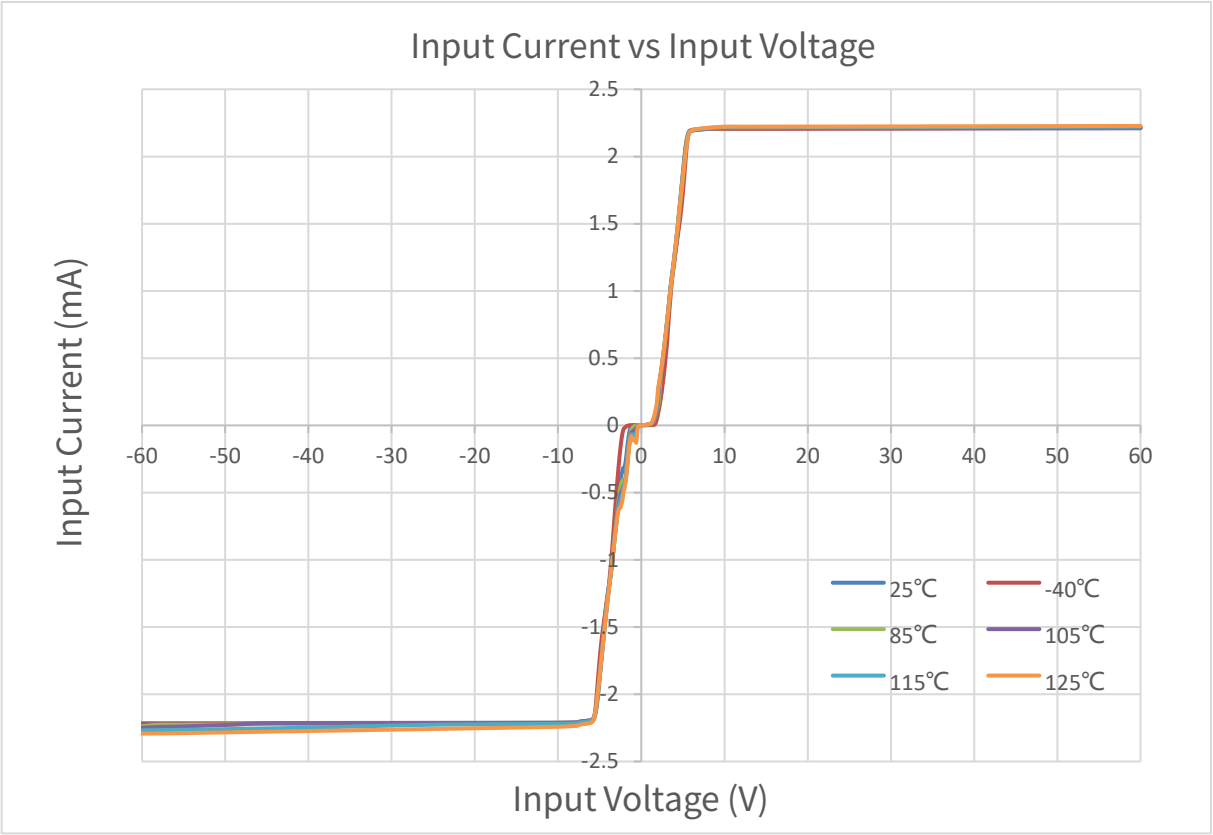


Figure 6.1 Input Current vs Input Voltage

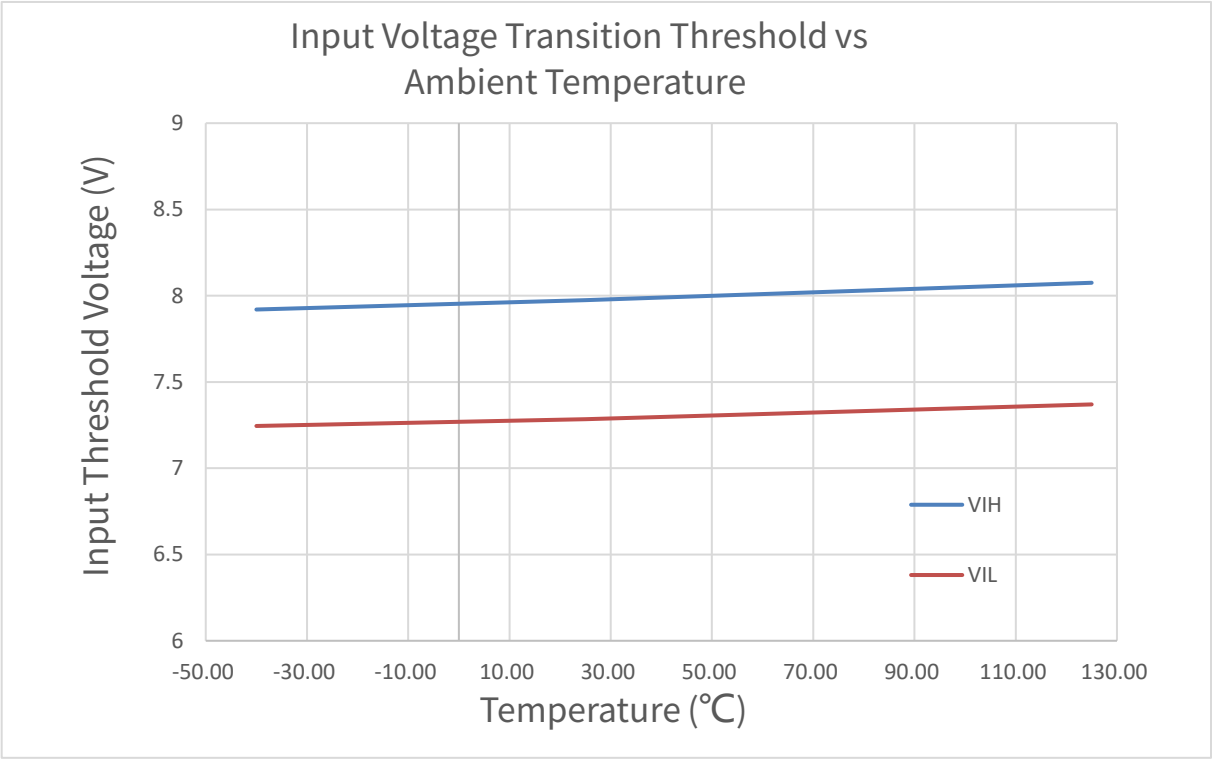


Figure 6.2 Input Voltage Transition Threshold vs Ambient Temperature

6.3. Parameter Measurement Information

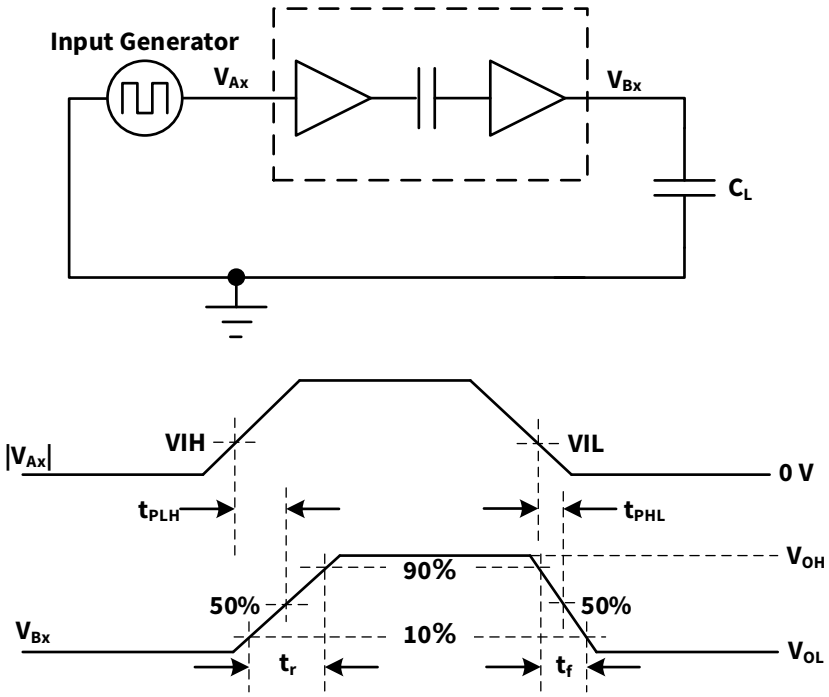


Figure 6.3 Switching Characteristics Test Circuit and Waveform

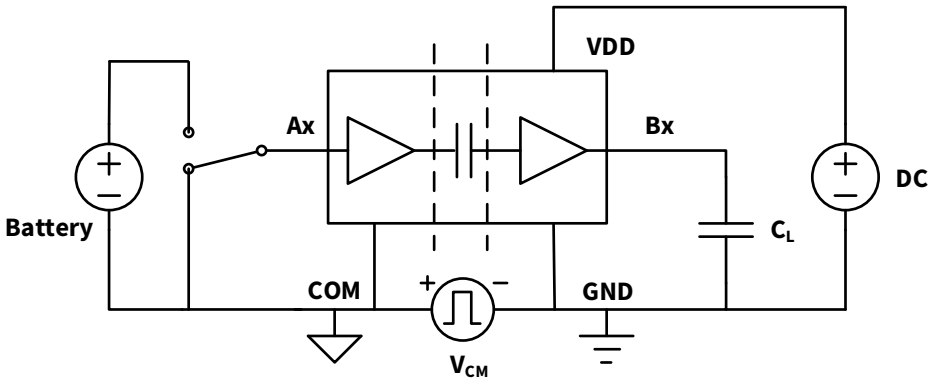


Figure 6.4 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value* SSOP20	*Unit*	*Comments*
Minimum External Clearance	CLR	3.9	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	3.9	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value* SSOP20
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to III
	For Rated Mains Voltage ≤ 300Vrms	I to II
	For Rated Mains Voltage ≤ 600Vrms	I
	For Rated Mains Voltage ≤ 1000Vrms	/
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value* SSOP20	*Unit*
Maximum repetitive isolation voltage		V_{IORM}	565	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	400	V_{RMS}
	DC Voltage		565	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\,(m)}$=1.5*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	5384	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	7000	V_{PEAK}

Description	Test Condition	Symbol	Value SSOP20	Unit
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	3000	V_{RMS}

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI8608-DSSTR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ =67.1 °C/W, T_J = 150 °C, T_A = 25 °C	1862	mW
Safety Supply Current	$R_{\theta JA}$ = 67.1 °C/ W, V_I = 5V, T_J = 150 °C, T_A = 25 °C	372	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SSOP20 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

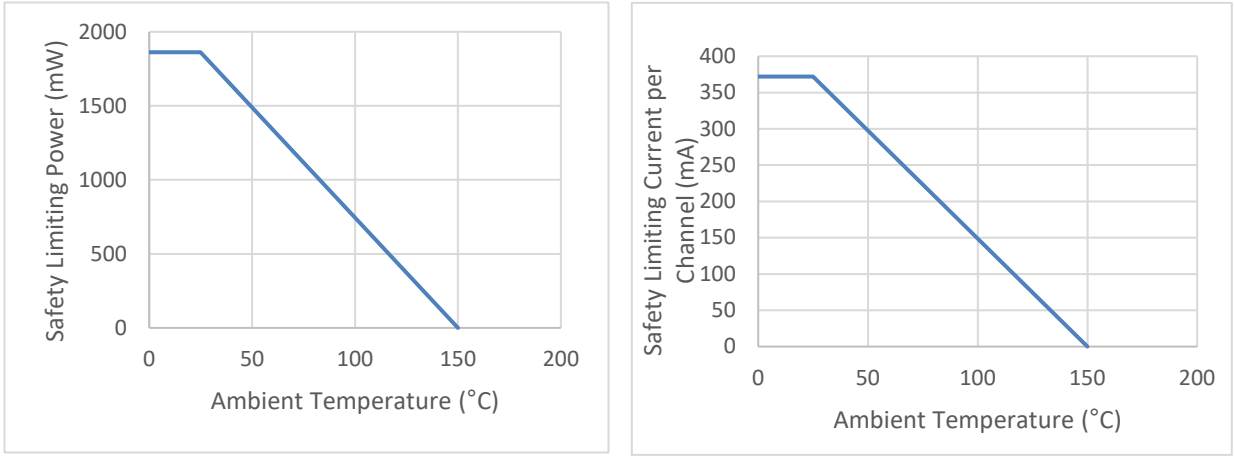


Figure 7.1 NSI8608-DSSTR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.4. Regulatory Information

The NSI8608-DSSTR is approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation V_{IORM}=565Vpeak V_{IOTM}=5000Vpeak V_{IOSM}=7000Vpeak	Basic insulation
E500602	E500602	File (pending)	File (CQC23001391251)

8. Function Description

8.1. Overview

The NSI8608 is fully-integrated, isolated digital-input receivers with IEC 61131-2 Type 1,2 and 3 characteristics. The device receives 24-V to 60-V digital-input signals and provide isolated digital outputs. Field-side input with no power supply supports sink and source current input through integrated rectifier bridge. The device integrates the current limiting function to effectively reduce the overall temperature of the solution. The voltage transition threshold is compliant with Type 1,2 and 3 and can be increased further using an external resistor. It can provide a transmission rate of 2Mbps and 380ns delay. The interface speed is much higher than that of traditional optocoupler schemes. It is more suitable for transmitting high-speed signals such as position feedback in electric drive applications.

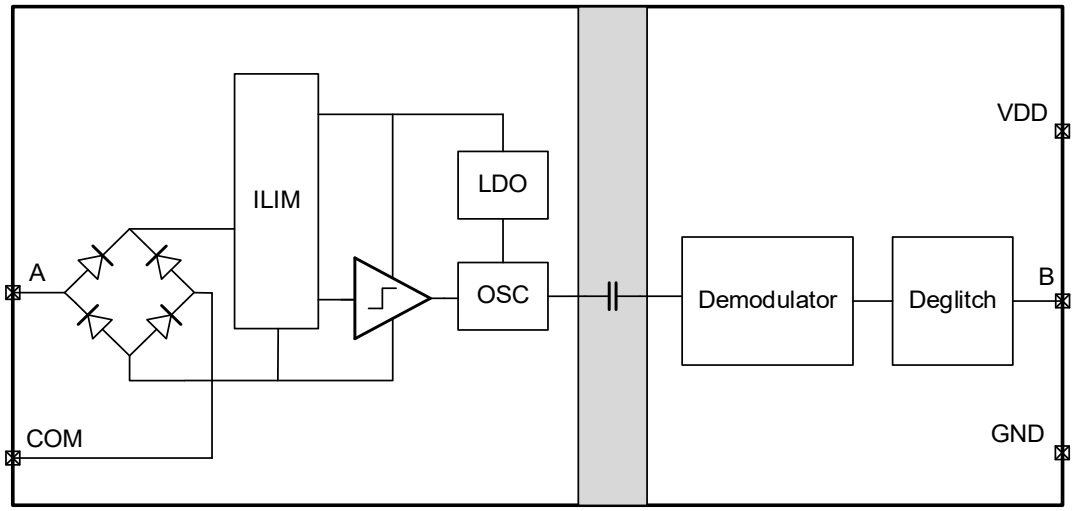


Figure 8.1 Functional Block Diagram

8.2. Feature Description

The NSI8608 supports up to ±60V digital signal inputs and provides isolated digital outputs. The current limiting function does not require any external device. Only one external resistor (R_{TH}) connected between the external input and Ax is used to adjust the input threshold. Refer to application note for more detail.

8.3. Device Functional Modes

Input (Ax)	*VDD status*	*Output (Bx)*	*Comment*
H	Ready	H	Normal operation.
L	Ready	L	
Open	Ready	L	
X	Unready	Undetermined	The output follows the same status with the input after output side VDD is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high			

8.4. OOK Modulation

NSI8608 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.8.2 & Fig.8.3, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

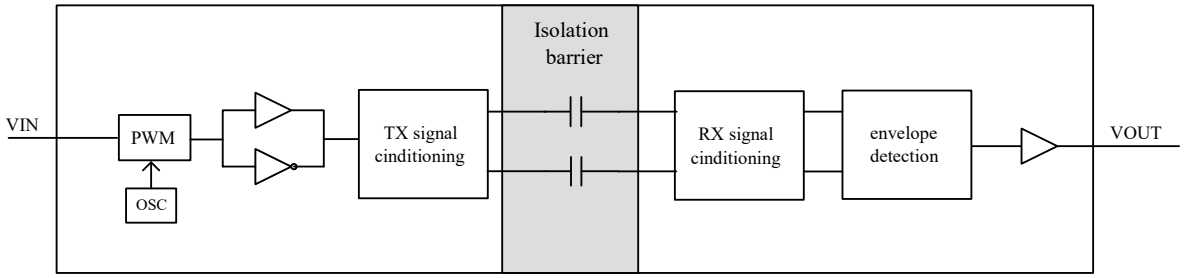


Figure 8.2 Single Channel Function Block Diagram

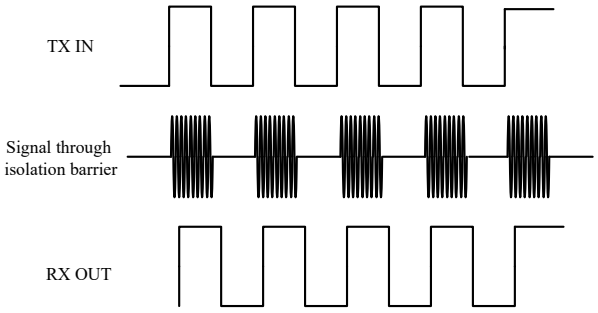


Figure 8.3 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

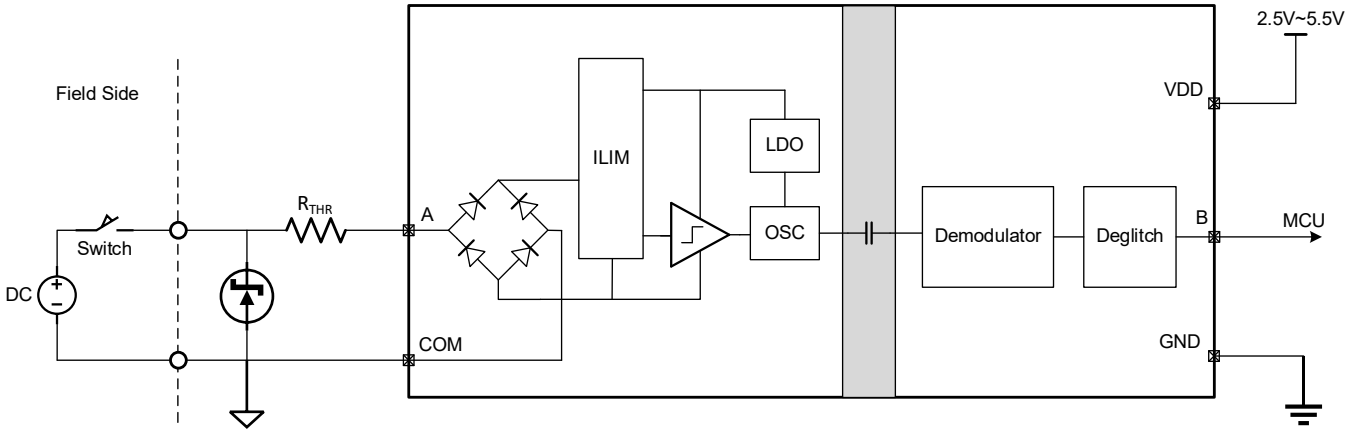


Figure 9.1 Typical isolation circuit for PLC

9.2. Thermal Considerations

Thermal considerations constrain operation at different input voltage level in Ax. The power dissipated inside the NSI8608 is determined by the voltage at the Ax pin (V_{Ax}) and the current drawn by the device (I_{Ax}). The internal power dissipated, when taken with the junction-to-air thermal resistance defined in the Thermal Information table can be used to determine the junction temperature for a given ambient temperature. The junction temperature must not exceed 150°C.

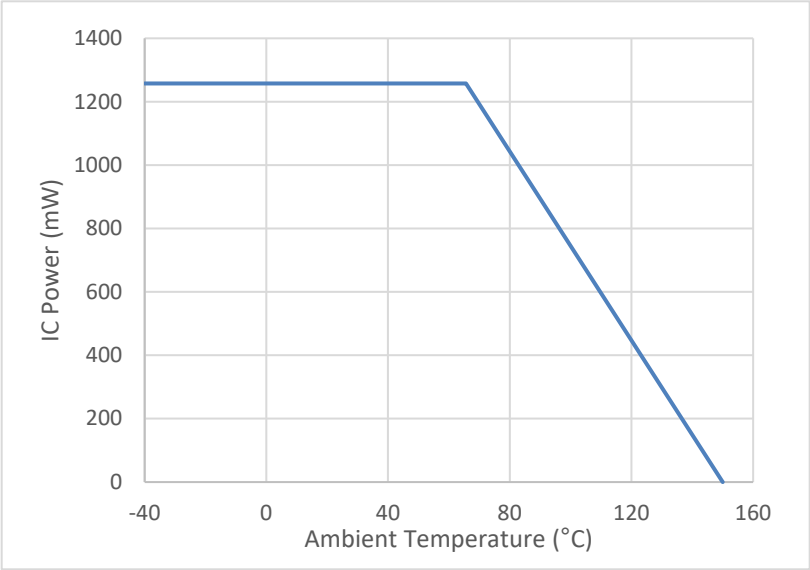


Figure 9.2 IC Power vs Ambient Temperature (°C)

9.3. PCB Layout

NSI8608 requires a 0.1 µF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. Make sure the space under the chip should keep free from planes, traces, pads and vias. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

On the field side, the sub pin must be kept floating.

The resistor (R_{TH}) connected between the external input and Ax is used to adjust the input threshold. The resistor connected between Ax and COM is used to adjust the input current. Refer to application note for more detail. The recommended device for TVS is SMAJ33CA. The capacitor connected between Ax and COM is not recommended in general. Figure 9.3 to Figure 9.4 show the recommended PCB layout.

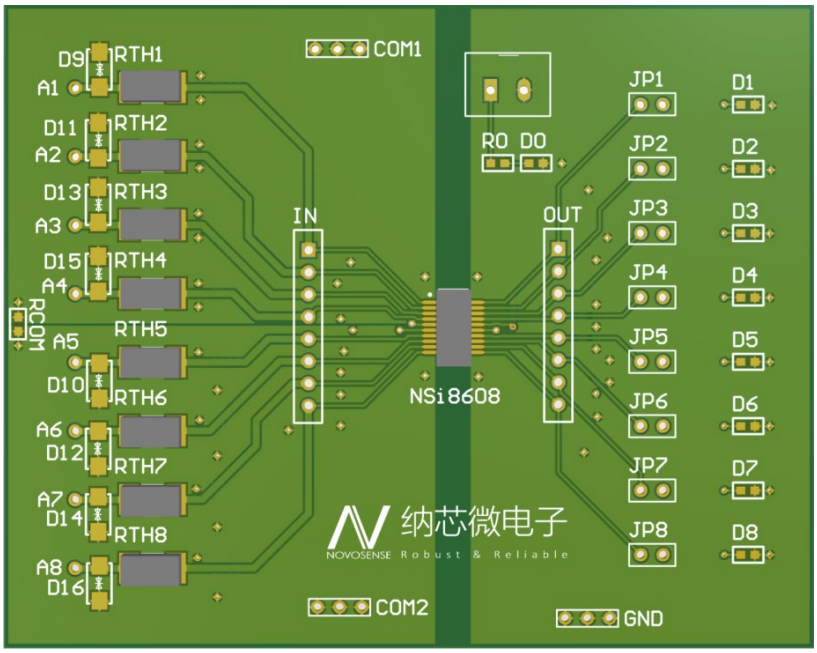


Figure 9.3 Recommended PCB Layout — Top Layer

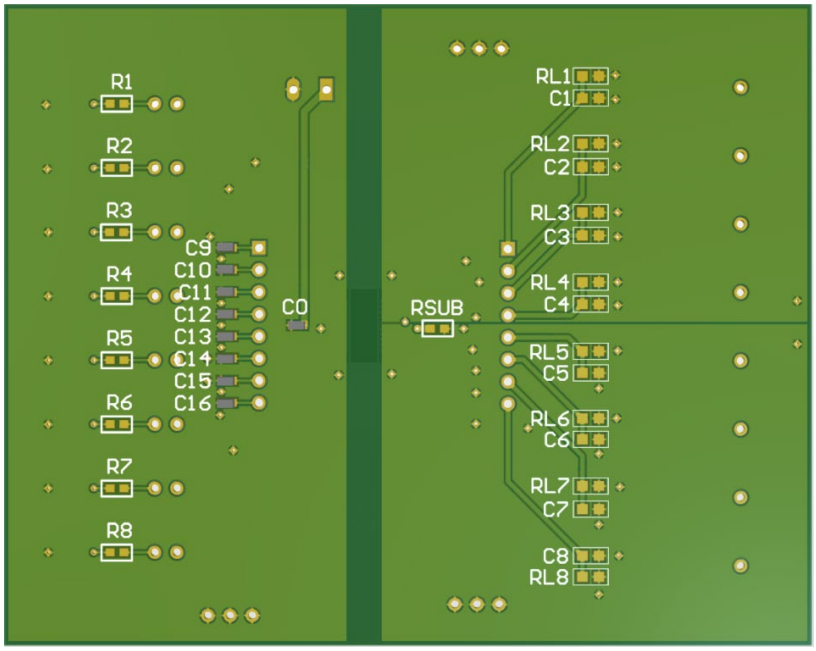
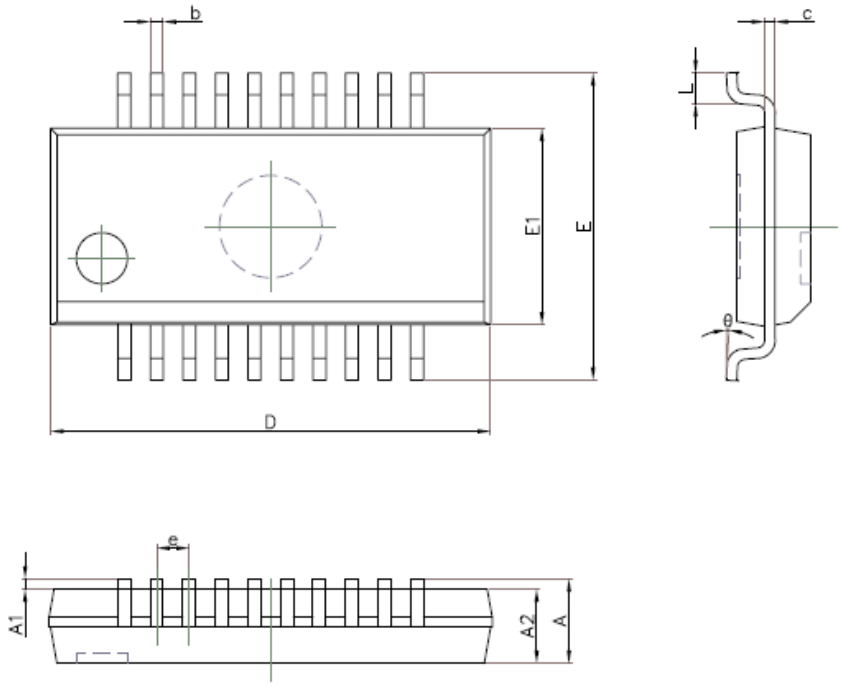


Figure 9.4 Recommended PCB Layout — Bottom Layer

10. Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.750	—	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	—	0.049	—
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SSOP20 Package Shape and Dimension in millimeters

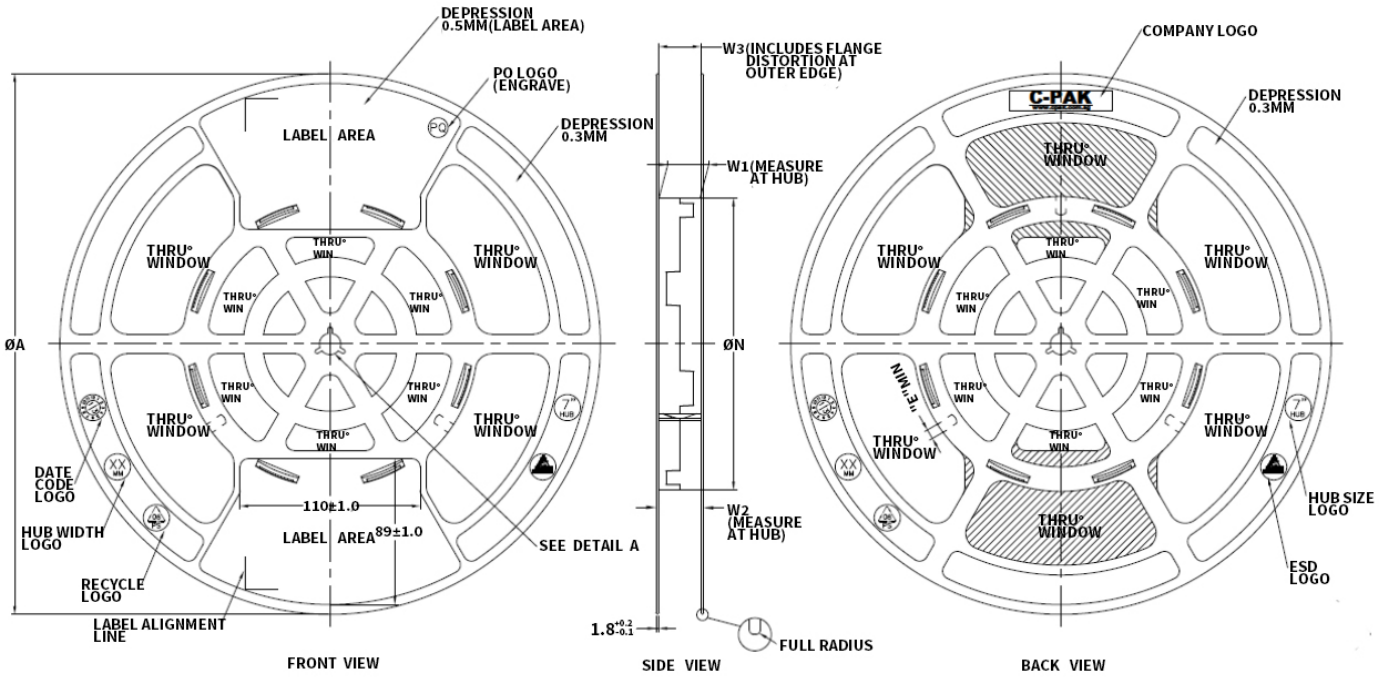
11. Ordering Information

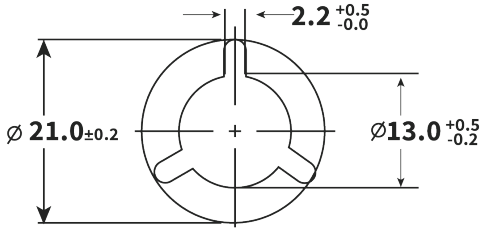
Part Number	*Isolation Rating (kV)*	*Number of inputs*	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSI8608-DSSTR	3	8	2	-40 to 125℃	2	SSOP20	SSOP20	2500

12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI8608	TBD	TBD	TBD	TBD

13. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)

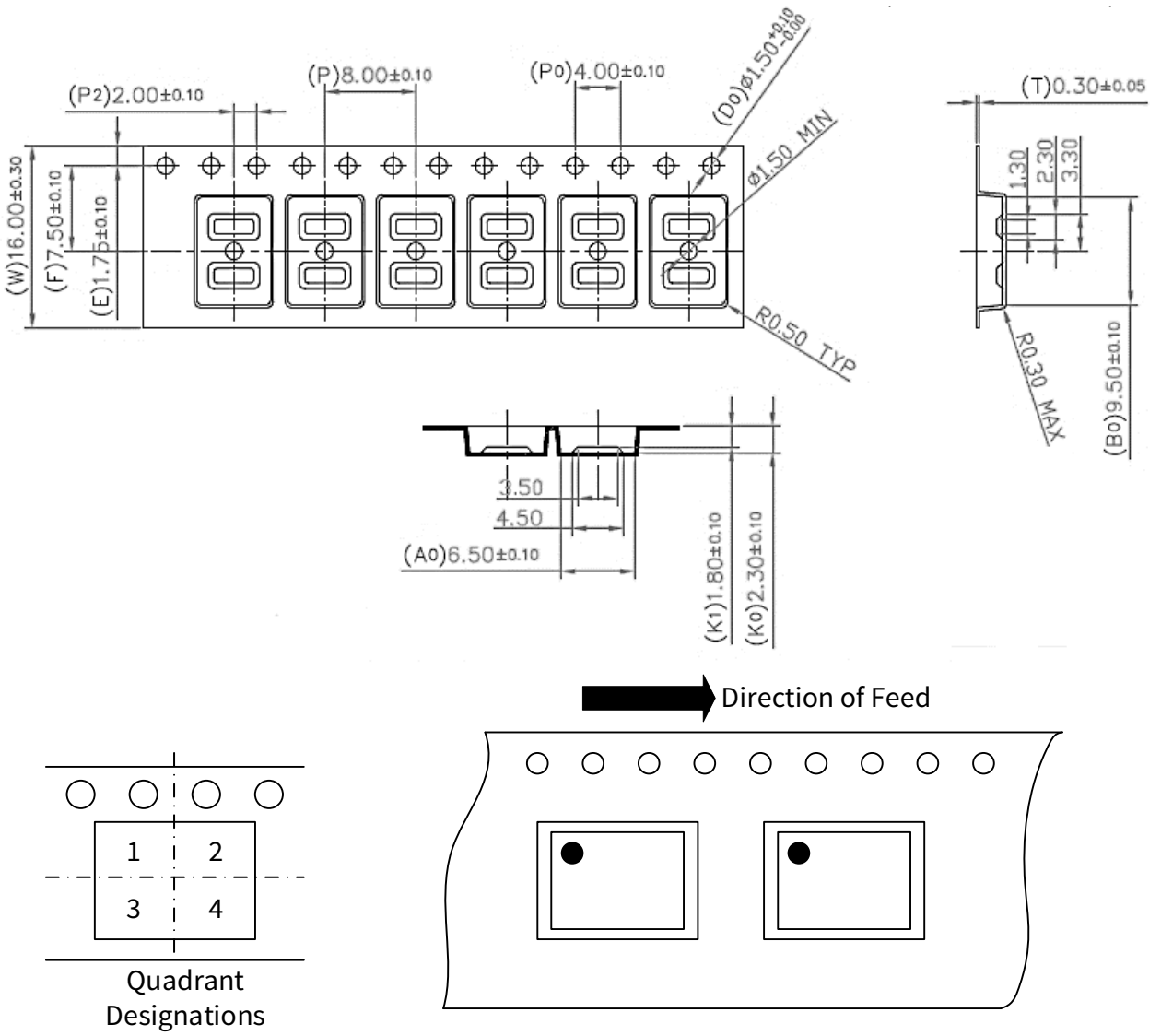


Figure 13.2 Tape Information of SSOP20

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/4/12

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