NCA9539-Q1

16-bit I²C-bus I/O port with interrupt and reset

Datasheet (EN) 1.2

Product Overview

The NCA9539-Q1 is a 24-pin device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for the two-line bidirectional I2C bus applications. The device can operate with a power supply voltage (V_{DD}) range from 1.65 V to 5.5 V. It provides a simple solution when additional I/Os are needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The NCA9539-Q1 consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The NCA9539-Q1 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. Also, the NCA9539-Q1 has a hardware RESET pin that can be used to reset the device to its default state.

The hardware pins (A0, A1) vary the fixed I2C-bus address and allow up to four devices to share the same I2C-bus.

Key Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- I2C to Parallel Port Expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current
- Open-drain active-low interrupt output
- Active-low reset input
- 5 V tolerant, 16 I/O ports which default to input mode
- Compatible with most microcontrollers
- Up to 400 kHz Fast I2C bus
- Noise filter on SCL/SDA inputs
- Polarity Inversion register
- Internal power-on reset
- No glitch on power-up
- Address by two hardware address pins for use of up to four devices
- Latched outputs with high-current drive capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22: 2000 V HBM and 1000 V CDM

Applications

- Automotive infotainment, ADAS, automotive body electronics, HEV, EV and powertrain
- Industrial automation, factory automation
- GPIO expansion for I2C-bus applications
- Servers, personal computers, personal electronics
- Routers (telecom switching equipment)
- Products with GPIO-Limited processors

Device Information

Part Number	*Package*	*Body Size*
NCA9539-Q1TSXR	TSSOP24	7.80mm*4.40mm

Pinout

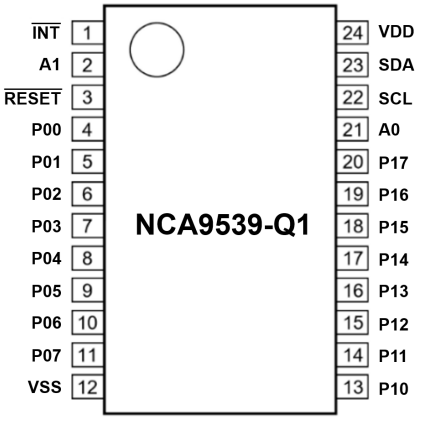

Figure 1. NCA9539-Q1 Pinout

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1. Pin Configuration and Functions

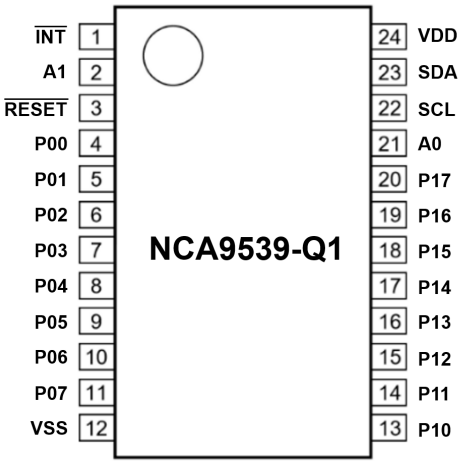


Figure 1-1. NCA9539-Q1 Package

Table 1-1. NCA9539-Q1 Pin Configuration and Description

SYMBOL	*PIN NO.*	*FUNCTION*
INT\	1	Interrupt open-drain output. Connect to VDD through a pull-up resistor
A1	2	Address input 1. Connect directly to VDD or ground
RESET\	3	Active-low reset input. Connect to VDD through a pull-up resistor
P00	4	Port 0 input/output. At power-on, the port is configured as an input
P01	5	
P02	6	
P03	7	
P04	8	
P05	9	
P06	10	
P07	11	
VSS	12	Ground
P10	13	Port 1 input/output. At power-on, the port is configured as an input
P11	14	
P12	15	
P13	16	

P14	17	
P15	18	
P16	19	
P17	20	
A0	21	Address input 0. Connect directly to VDD or ground
SCL	22	Serial clock bus. Connect to VDD through a pull-up resistor
SDA	23	Serial data bus. Connect to VDD through a pull-up resistor
VDD	24	Supply voltage

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1].

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Comments*
Supply voltage	V_{DD}	-0.5	6.0	V	
Voltage on an input/output pin	$V_{I/O}$	-0.5	6.0	V	
Output current	I_O	-	±50	mA	
Input current	I_I	-	±20	mA	
Supply current	I_{DD}	-	160	mA	
Ground supply current	I_{SS}	-	200	mA	
Total power dissipation	P_{tot}	-	200	mW	
Junction temperature	T_J	-	135	°C	
Storage temperature	T_{stg}	-65	150	°C	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

3. EMC Ratings

Parameters	*Ratings*	*Value*	*Unit*
Electrostatic discharge	Human Body Model (HBM), per ANSI/ ESDA/ JEDEC JS-001 ● All pins	±6	kV
	Charged Device Model (CDM), per ANSI/ ESDA/ JEDEC JS-002 ● All pins	±1	kV

4. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Supply voltage	V_{DD}	1.65	5.5	V
High-level input voltage	V_{IH}	0.7*V_{DD}	5.5	V
Low-level input voltage	V_{IL}	-0.5	0.3*V_{DD}	V
High-level output current (IO port)	I_{OH}		-10	mA
Low-level output current (IO port)	I_{OL}		10	mA
Low-level output current (INT\, SDA)	I_{OL}		3.5	mA
Operating free-air temperature	T_A	-40	125	°C

5. Thermal Characteristics

Parameters	*Symbol*	*TSSOP24*	*Unit*
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	108.8	°C /W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	54	°C /W
Junction-to-board thermal resistance	$R_{\theta JB}$	62.8	°C /W

6. Specifications

6.1. Electrical Characteristics

V_{DD}= 1.65V to 5.5V; T_{amb} = -40°C to 125°C; V_I is the voltage on I/O port; unless otherwise noted.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Input diode clamp voltage	V_{IK}	-1.2	-	-	V	I_I=-18mA
Supplies						
Supply voltage Range	V_{DD}	1.65	-	5.5	V	
Supply current	I_{DD}	-	25.8	70	μA	Operating mode; V_{DD} = 5.5 V; I/O=input; V_I=V_{DD}; no load; f_{SCL} = 400 kHz
		-	10.3	30	μA	Operating mode; V_{DD} = 3.3 V; I/O=input; V_I=V_{DD}; no load; f_{SCL} = 400 kHz
		-	3.5	9	μA	Operating mode; V_{DD} = 1.65 V; I/O=input; V_I=V_{DD}; no load; f_{SCL} = 400 kHz
Standby current	I_{stb}	-	0.18	9	μA	Standby mode; V_{DD} = 5.5 V; I/O=input; V_I=V_{DD}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
		-	0.10	5	μA	Standby mode; V_{DD} = 3.3 V; I/O=input; V_I=V_{DD}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
		-	0.04	2.5	μA	Standby mode; V_{DD} = 1.65 V; I/O=input; V_I=V_{DD}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
		-	0.25	20	μA	Standby mode; V_{DD} = 5.5 V; I/O=input; V_I=V_{SS}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
		-	0.10	13	μA	Standby mode; V_{DD} = 3.3 V; I/O=input; V_I=V_{SS}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
		-	0.04	5.5	μA	Standby mode; V_{DD} = 1.65 V; I/O=input; V_I=V_{SS}; no load; V_I = V_{SS}; f_{SCL} = 0 kHz
Power On Reset Voltage, Rising[1]	V_{PORR}	0.75	1.17	1.5	V	no load; VI = V_{DD} or V_{SS}
Power On Reset Voltage, Falling[1]	V_{PORF}	0.75	1.05	1.5	V	no load; VI = V_{DD} or V_{SS}
Input SCL; Input and Output SDA						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{DD}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{DD}	-	5.5	V	

LOW-level output current	I_{OL}	3	-	-	mA	V_{DD} = 1.65 V to 5.5 V; V_{OL} = 0.4 V
Input leakage current	I_L	-1	-	1	μA	V_{DD} = 1.65V to 5.5 V; V_I = V_{DD} or V_{SS}
Input capacitance	C_i	-	6	10	pF	V_I = V_{SS}
I/Os						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{DD}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{DD}	-	5.5	V	
LOW-level output current	I_{OL}	8	-	-	mA	V_{DD} = 1.65 V to 5.5 V; V_{OL} = 0.3 V[2]
		10	-	-	mA	V_{DD} = 1.65 V to 5.5 V; V_{OL} = 0.35 V[2]
HIGH-level output voltage	V_{OH}	1.2	-	-	V	I_{OH} = -8 mA; V_{DD} = 1.65 V[3]
		1.0	-	-	V	I_{OH} = -10 mA; V_{DD} = 1.65 V[3]
		1.7	-	-	V	I_{OH} = -8 mA; V_{DD} = 2.3 V[3]
		1.4	-	-	V	I_{OH} = -10 mA; V_{DD} = 2.3 V[3]
		2.5	-	-	V	I_{OH} = -8 mA; V_{DD} = 3.0 V[3]
		2.4	-	-	V	I_{OH} = -10 mA; V_{DD} = 3.0 V[3]
		3.3	-	-	V	I_{OH} = -8 mA; V_{DD} = 3.6V[3]
		3.2	-	-	V	I_{OH} = -10 mA; V_{DD} = 3.6V[3]
		5.1	-	-	V	I_{OH} = -8 mA; V_{DD} = 5.5 V[3]
		5.0	-	-	V	I_{OH} = -10 mA; V_{DD} = 5.5 V[3]
HIGH-level input leakage current	I_{LIH}	-	-	1	μA	V_{DD} = 5.5 V; V_I = V_{DD}
LOW-level input leakage current	I_{LIL}	-	-	-1	μA	V_{DD} = 5.5 V; V_I = V_{SS}
Input capacitance	C_i	-	3.7	9.5	pF	
Output capacitance	C_o	-	3.7	9.5	pF	
Interrupt $\overline{INT}$						
LOW-level output current	I_{OL}	3	-	-	mA	V_{DD} = 1.65 V to 5.5 V; V_{OL}=0.4V

Select Inputs A0, A1						
LOW-level input voltage	V_{IL}	-0.5	-	$0.3*V_{DD}$	V	
HIGH-level input voltage	V_{IH}	$0.7*V_{DD}$	-	5.5	V	
Input leakage current	I_{LI}	-1	-	1	μA	V_{DD} = 1.65 V to 5.5 V; V_I = V_{DD} or V_{SS}
$\overline{RESET}$						
Input leakage current	I_{LI}	-1	-	1	μA	V_{DD} = 1.65 V to 5.5 V; RESET = V_{DD} or V_{SS}

1. V_{DD} must be lowered to 0.2V for at least 50μs in order to reset part.

2. Each I/O must be externally limited to a maximum of 25 mA and each octal (P00 to P07 and P10 to P17) must be limited to a maximum current of 100 mA for a device total of 200 mA.

3. The total current sourced by all I/Os must be limited to 160 mA.

6.2. Dynamic Characteristics

V_{DD}= 1.65V to 5.5V; T_{amb} = -40°C to 125°C; unless otherwise noted.

Parameters	*Symbol*	*Standard-mode I2C-bus*		*Fast-mode I2C-bus*		*Unit*
		Min	*Max*	*Min*	*Max*	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	0.6	-	µs
set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
data valid acknowledge time	$t_{VD;ACK}$[1]	0.3	3.45	0.1	0.9	µs
data hold time	$t_{HD;DAT}$	0	-	0	-	ns
data valid time	$t_{VD;DAT}$[2]	300	-	50	-	ns
data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$[3]	300	ns
rise time of both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b$[3]	300	ns
pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	50	-	50	ns
reset pulse width	$t_{w(rst)}$	6	-	6	-	ns
reset recovery time	$t_{rec(rst)}$	200	-	200	-	ns
reset time	t_{rst}	400	-	400	-	ns
data output valid time	$t_{v(Q)}$	-	300	-	300	ns
data input set-up time	$t_{su(D)}$	150	-	150	-	ns
data input hold time	$t_{h(D)}$	1	-	1	-	µs
valid time on pin /INT	$t_{v(INT\_N)}$ [4]	-	4	-	4	µs
reset time on pin /INT	$t_{rst(INT\_N)}$ [5]	-	4	-	4	µs

1. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW, see Figure 6-2.
2. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW, see Figure 6-2.
3. C_b = total capacitance of one bus line in pF.

4. $t_{V(INT\_N)}$ is measured from 50% IO input to 0.3*V_{DD} on INT\
5. $t_{rst(INT\_N)}$ is measured from 0.3*V_{DD} on SCL to 0.7*V_{DD} on INT\.

6.3. Parameter Measurement Information

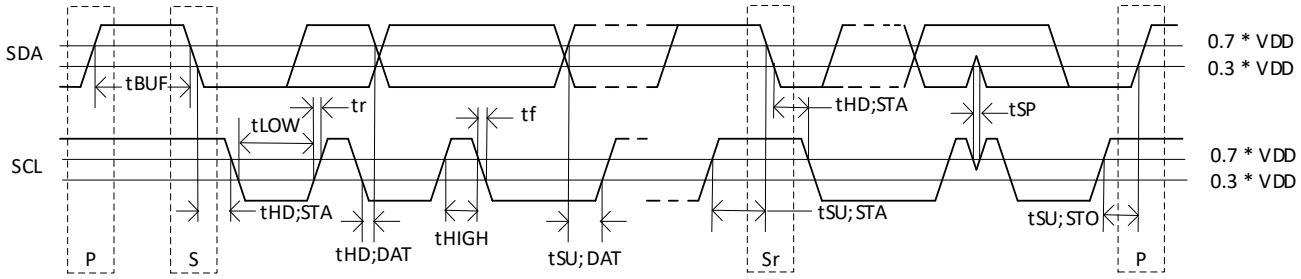


Figure 6-1. Definition of timing on I^2C-bus

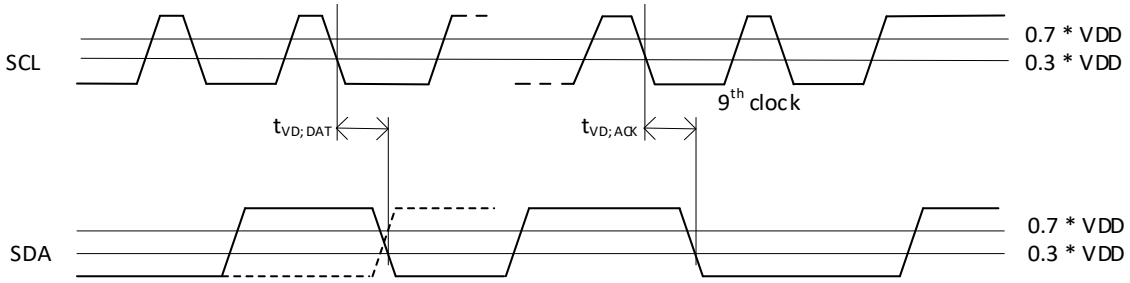


Figure 6-2. Parameter Measurement Waveform: $t_{VD;DAT}$ & $t_{VD;ACK}$

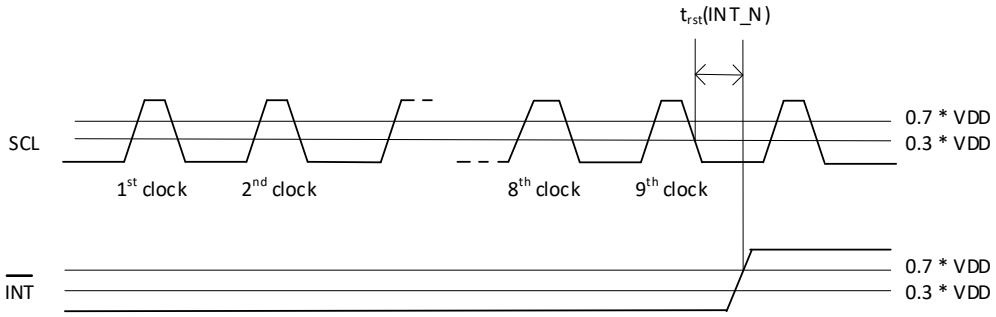


Figure 6-3. Parameter Measurement Waveform: $t_{rst(INT\_N)}$

7. Detailed Description

7.1. Functional Block Diagram

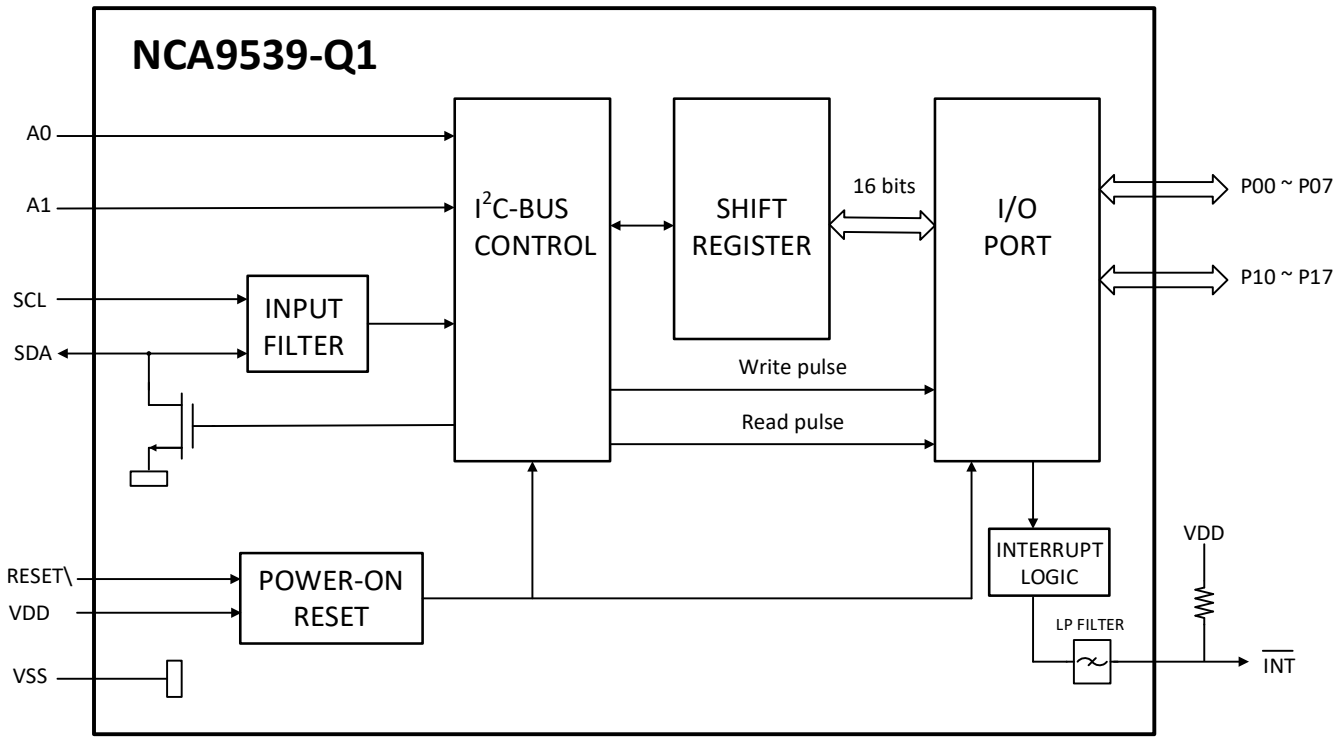


Figure 7-1. Block Diagram of NCA9539-Q1

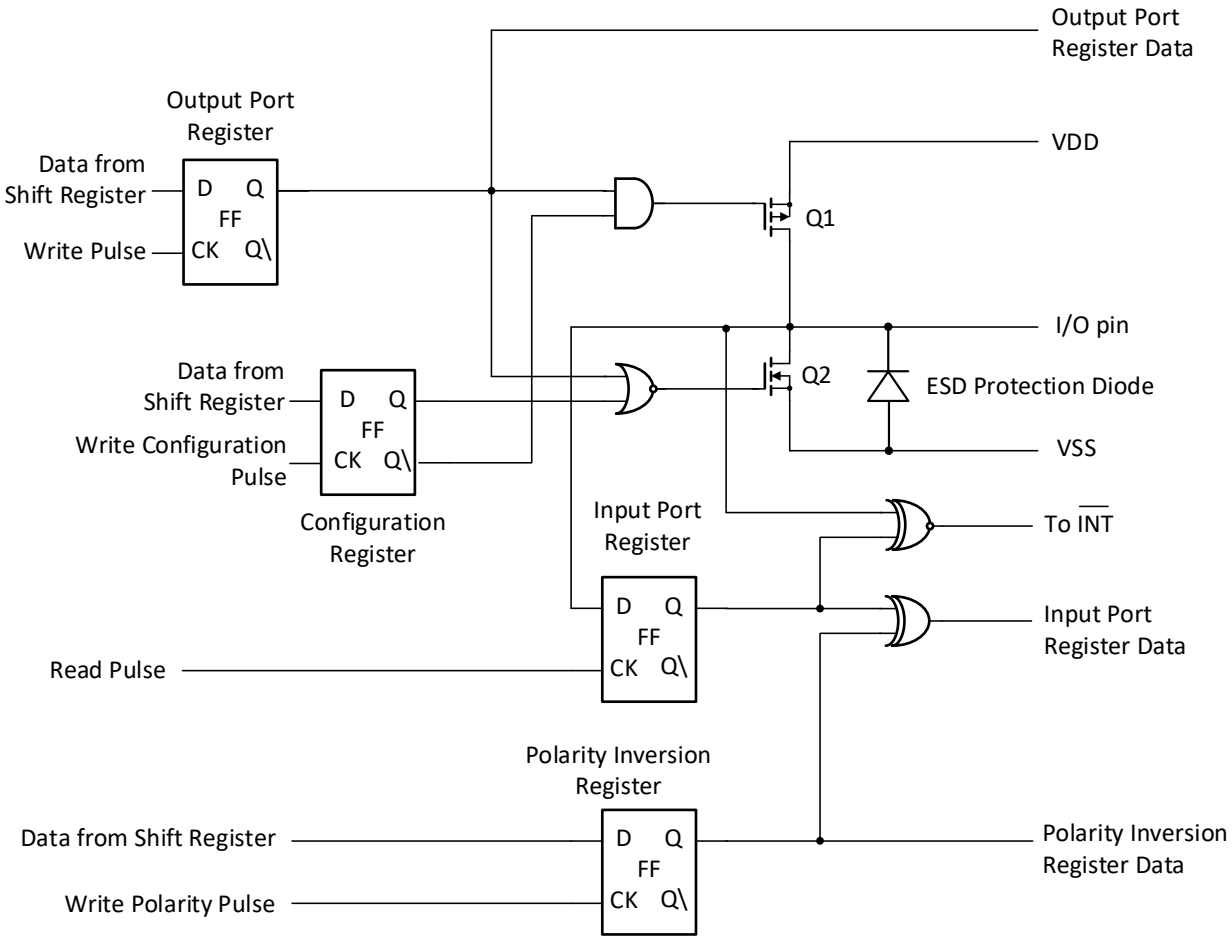


Figure 7-2. Simplified schematic of I/Os

7.2. Feature description

7.2.1. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VDD or VSS.

7.2.2. RESET\ input

A reset can be accomplished by holding the RESET\ pin low for a minimum of t_w. The NCA9539-Q1 registers and I2C state machine are held in their default states until RESET\ is once again high. This input requires a pull-up resistor to VDD, if no active connection is used.

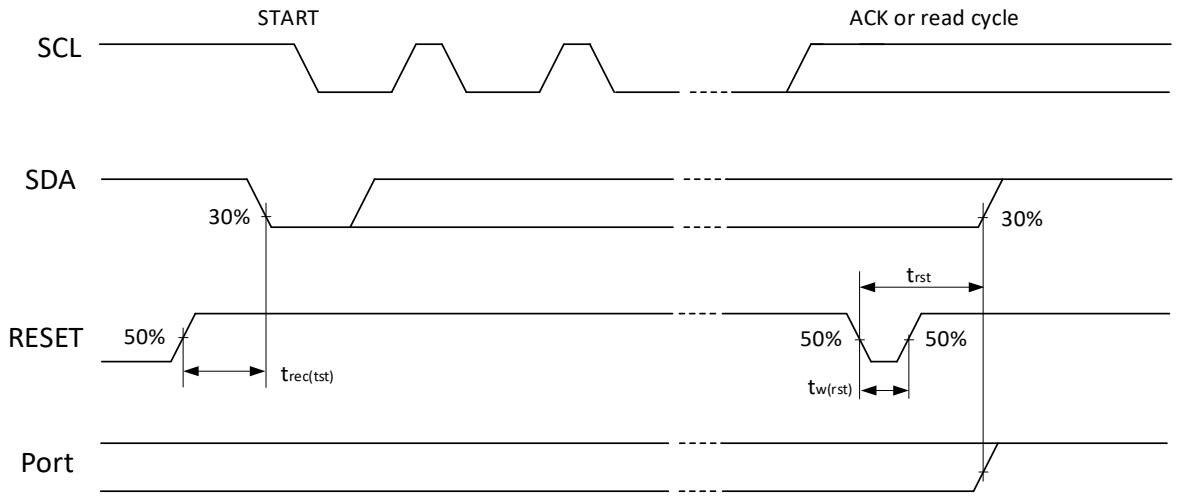


Figure 7-3. Definition of RESET\ timing

7.2.3. Interrupt (INT\ ) Output

An interrupt is activated at any rising or falling edge of the port inputs changing state in the input mode. After time, t_{iv}, the signal INT\ is valid. The interrupt is deactivated when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Each change of the I/Os after resetting is detected and is transmitted as INT\.

Since each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa. Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

INT\ has an open-drain structure and requires a pull-up resistor to VDD.

7.3. Device functional modes

7.3.1. Power-On Reset

When power is applied to VDD, an internal power-on reset holds the NCA9539-Q1 in a reset condition until VDD has reached V_{POR}. At that point, the reset condition is released and the NCA9539-Q1 registers and I2C state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V for at least 50µs.

7.4. Programming

7.4.1. I2C Interface

The NCA9539-Q1 has a standard bidirectional I2C interface that is controlled by a master device in order to be configured or read the status of this device.

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. The size of the pull-up resistor is determined by the amount of capacitance on the I2C lines. Data transfer may be initiated only when the bus is idle.

Each slave on the I2C bus has a specific device address to differentiate between other slave devices that are on the same I2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The general procedure for a master to access a slave device is as below.

1. If a master wants to send data to a slave:

• Master-transmitter sends a START condition and addresses the slave-receiver.

• Master-transmitter sends data to slave-receiver.

• Master-transmitter terminates the transfer with a STOP condition.

2. If a master wants to receive or read data from a slave:

• Master-receiver sends a START condition and addresses the slave-transmitter.

• Master-receiver sends the requested register to read to slave-transmitter.

• Master-receiver receives data from the slave-transmitter.

• Master -receiver terminates the transfer with a STOP condition.

Note: MSB first in data transfer.

7.4.2. Start and Stop Conditions

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

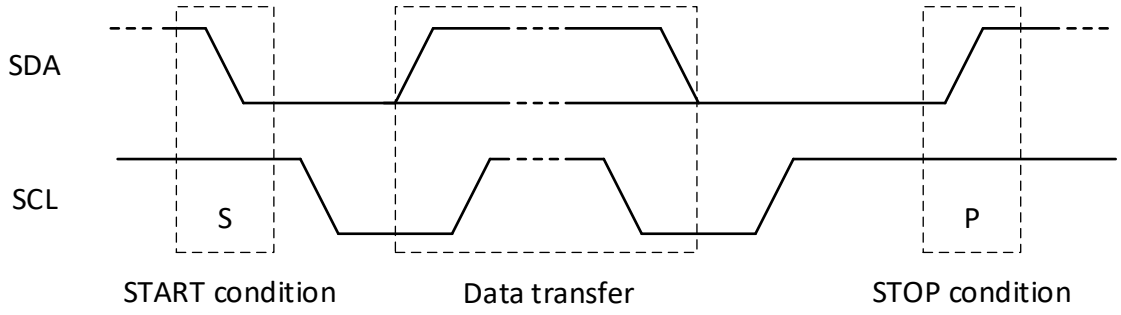


Figure 7-4. Definition of START and STOP conditions

7.4.3. Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

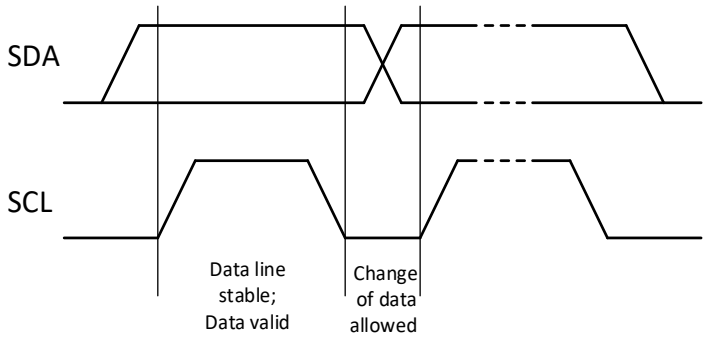


Figure 7-5. Bit transfer

7.4.4. System Configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 7-6).

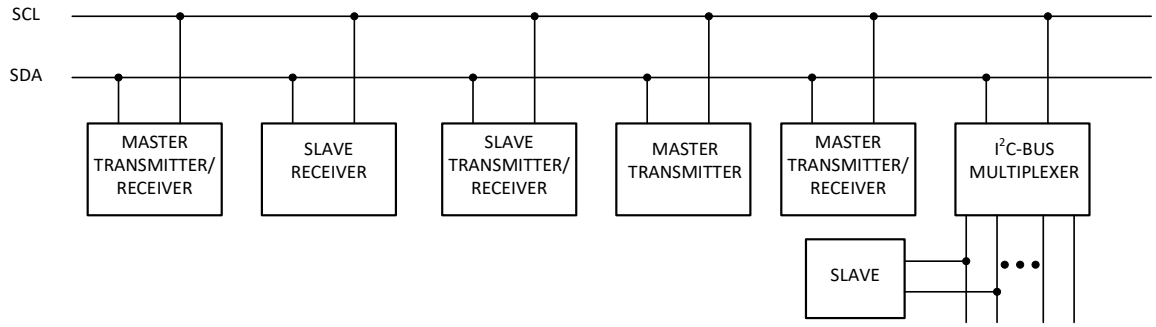


Figure 7-6. System configuration

7.4.5. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. In the same way, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

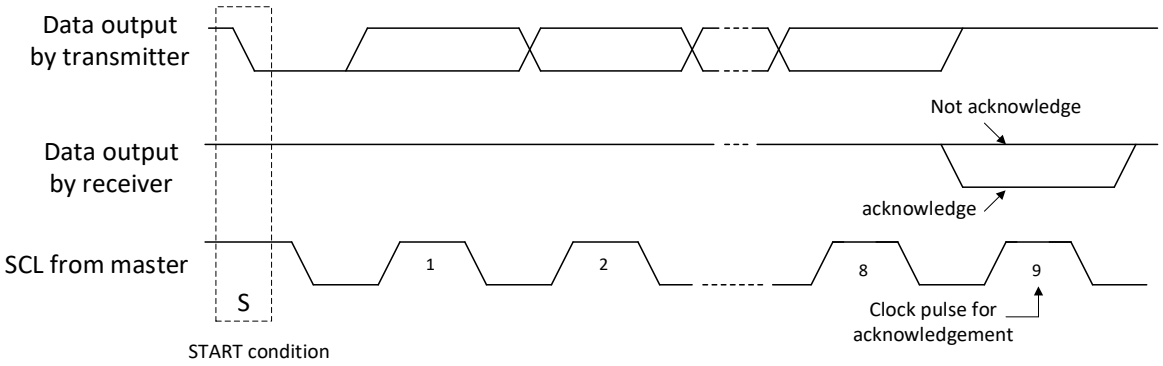


Figure 7-7. Acknowledgement on I^2C-bus

7.5. Register Maps

The register maps of the NCA9539-Q1 include input port registers, output port registers, polarity inversion port registers and configuration registers.

7.5.1. Device Address

Figure 7-8 shows the address byte of the NCA9539-Q1. The last bit of the target address defines the operation (read or write) to be performed. A HIGH (1) selects a read operation, while a LOW (0) selects a write operation.

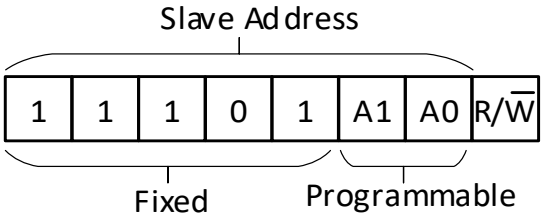


Figure 7-8. NCA9539-Q1 device address

Table 7-1 shows the address reference of the NCA9539-Q1.

Table 7-1. Address Reference

Inputs		I2C Bus Slave Address
A1	A0	
L	L	116(decimal), 74h(hexadecimal)
L	H	117(decimal), 75h(hexadecimal)
H	L	118(decimal), 76h(hexadecimal)
H	H	119(decimal), 77h(hexadecimal)

7.5.2. Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte shown in Table 7-2 that is stored in the write-only control register in the NCA9539-Q1. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that is affected. The command byte is sent only during a write transmission. Figure 7-9 shows the control register bits.

The bits written to the chip registers through the I2C protocol takes effect after the rising edge of the ACK clock, following a delay of tv(Q). Therefore, it is recommended to write to registers 6 and 7 (configuration registers) after registers 2 and 3 (output registers) as well as registers 4 and 5 (polarity inversion registers), in order to avoid errors on the I/O ports.

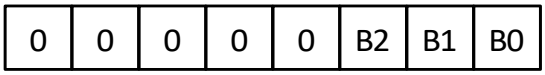


Figure 7-9. NCA9539-Q1 control register bits

Table 7-2. Command byte

Control Register Bits			Command Byte Hex	Register	Protocol	Power-up Default
B2	B1	B0				
0	0	0	00h	Input port 0	Read byte	1111 1111
0	0	1	01h	Input port 1	Read byte	1111 1111
0	1	0	02h	Output port 0	Read/write byte	1111 1111
0	1	1	03h	Output port 1	Read/write byte	1111 1111
1	0	0	04h	Polarity inversion port 0	Read/write byte	0000 0000
1	0	1	05h	Polarity inversion port 1	Read/write byte	0000 0000
1	1	0	06h	Configuration port 0	Read/write byte	1111 1111
1	1	1	07h	Configuration port 1	Read/write byte	1111 1111

7.5.3. Registers 0 and 1: Input port register pair

This register pair is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Registers 6 and 7. Writing to this register pair has no effect.

Table 7-3. Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	1	1	1	1	1	1	1	1

Table 7-4. Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	1	1	1	1	1	1	1	1

7.5.4. Registers 2 and 3: Output port registers

This register pair is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register pair have no effect on pins defined as inputs. In turn, reading from this register reflects the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7-5. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 7-6. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

7.5.5. Registers 4 and 5: Polarity inversion registers

This register pair allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with 1), the corresponding input port pin's polarity is inverted. If a bit in this register is cleared (written with 0), the corresponding input port pin's original polarity is retained.

Table 7-7. Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 7-8. Polarity Inversion Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

7.5.6. Registers 6 and 7: Configuration registers

This register pair configures the directions of the I/O pins. If a bit in this register is set (written with 1), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with 0), the corresponding port pin is enabled as an output.

Table 7-9. Configuration Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 7-10. Configuration Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

7.6. Bus Transactions

7.6.1.Writing to the Port Registers

Data is transmitted to the NCA9539-Q1 by sending the device address and setting the least significant bit to a logic 0 (see Figure 7-8). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the NCA9539-Q1 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 7-10 and Figure 7-11). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

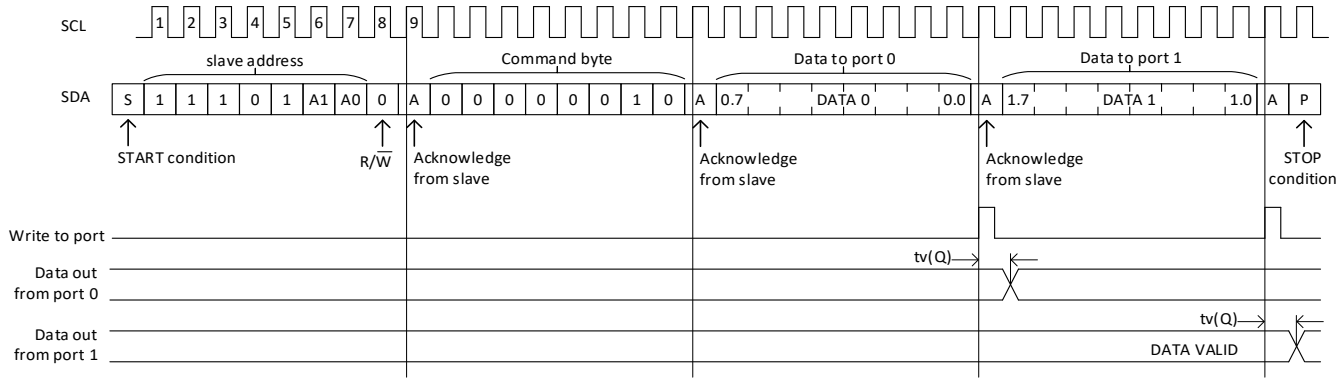


Figure 7-10. Write to output port registers

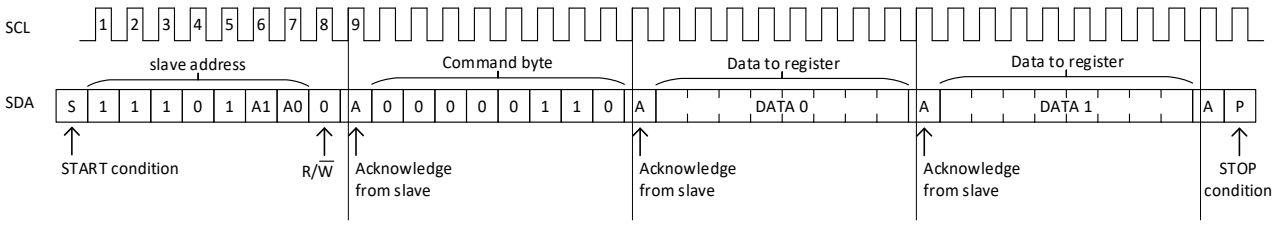
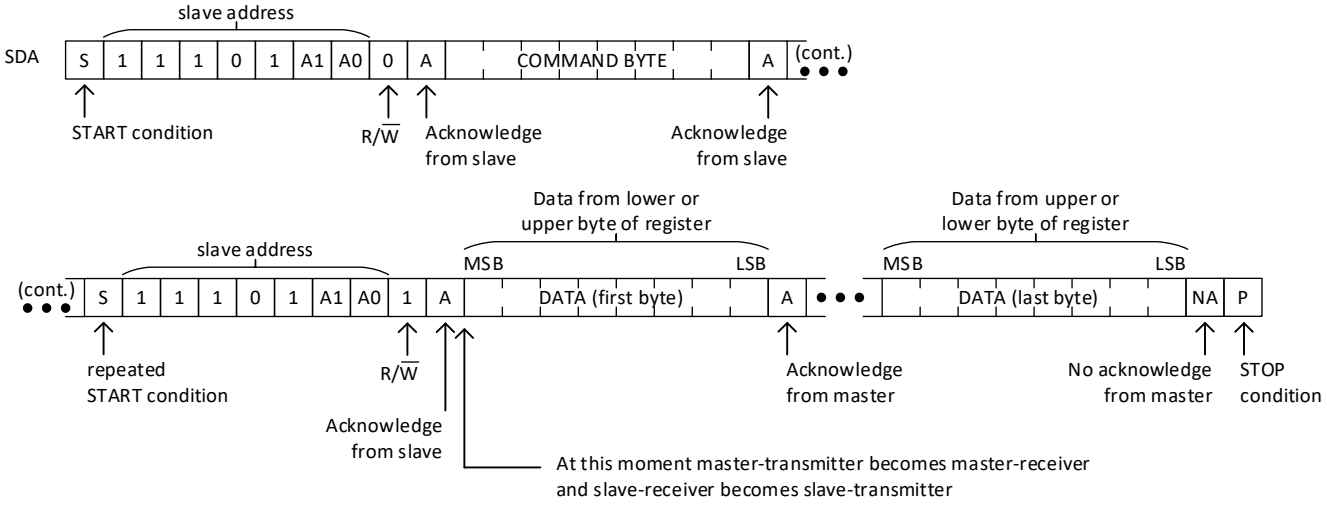


Figure 7-11. Write to config registers

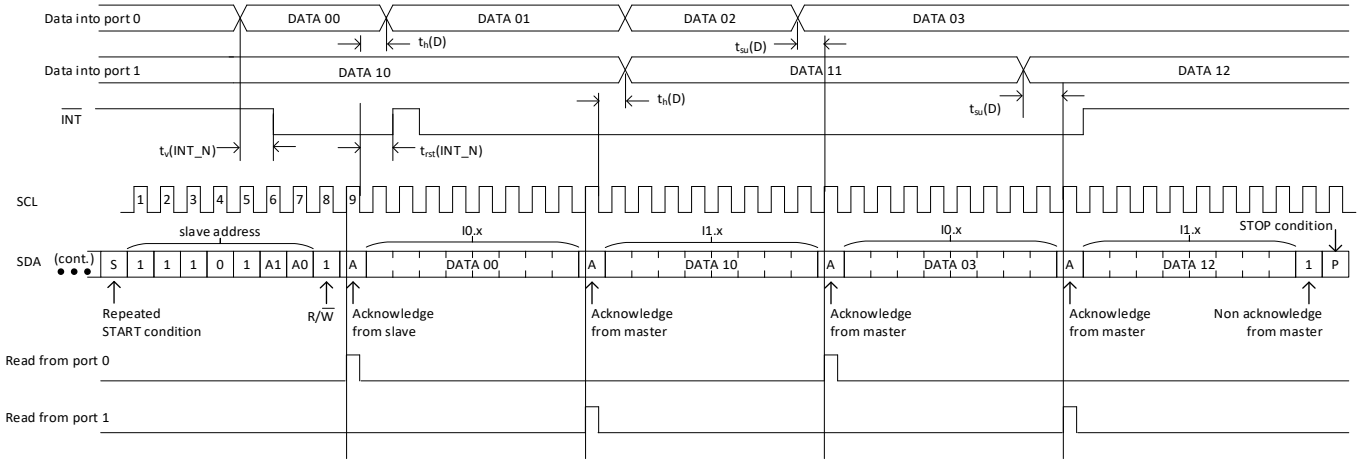
7.6.2. Reading the Port Registers

In order to read data from the NCA9539-Q1, the bus master must first send the NCA9539-Q1 address with the least significant bit set to a logic 0 (see Figure 7-8). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the NCA9539-Q1 (see Figure 7-12, Figure 7-13 and Figure 7-14). Data is clocked into the register on the rising edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if Input Port 1 is read, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission, but the final byte received, the bus master must not acknowledge the data.



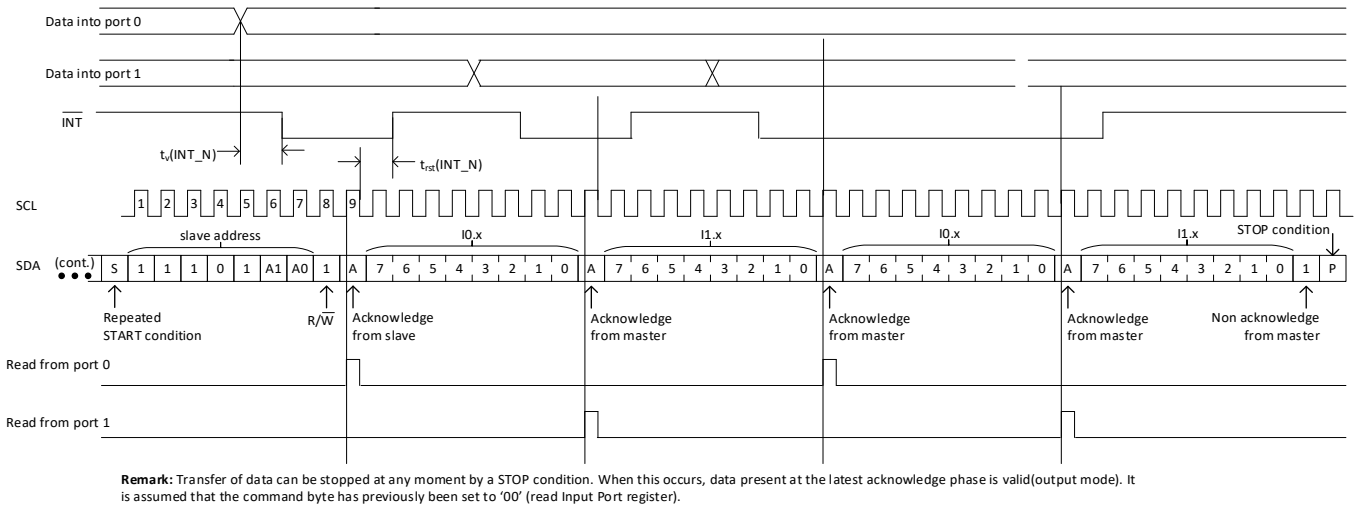
Remark: Transfer of data can be stopped at any moment by a STOP condition.

Figure 7-12. Read from registers



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid(output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 7-13. Read input port registers, scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid(output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 7-14. Read input port registers, scenario 2

8. Application Design-In Information

8.1. Application Information

In applications of the NCA9539-Q1, the device is connected as a slave to an I2C controller (processor), and the I2C bus may contain any number of other slave devices. The NCA9539-Q1 is typically in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

IO Expanders such as the NCA9539-Q1 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

8.2. Typical Application

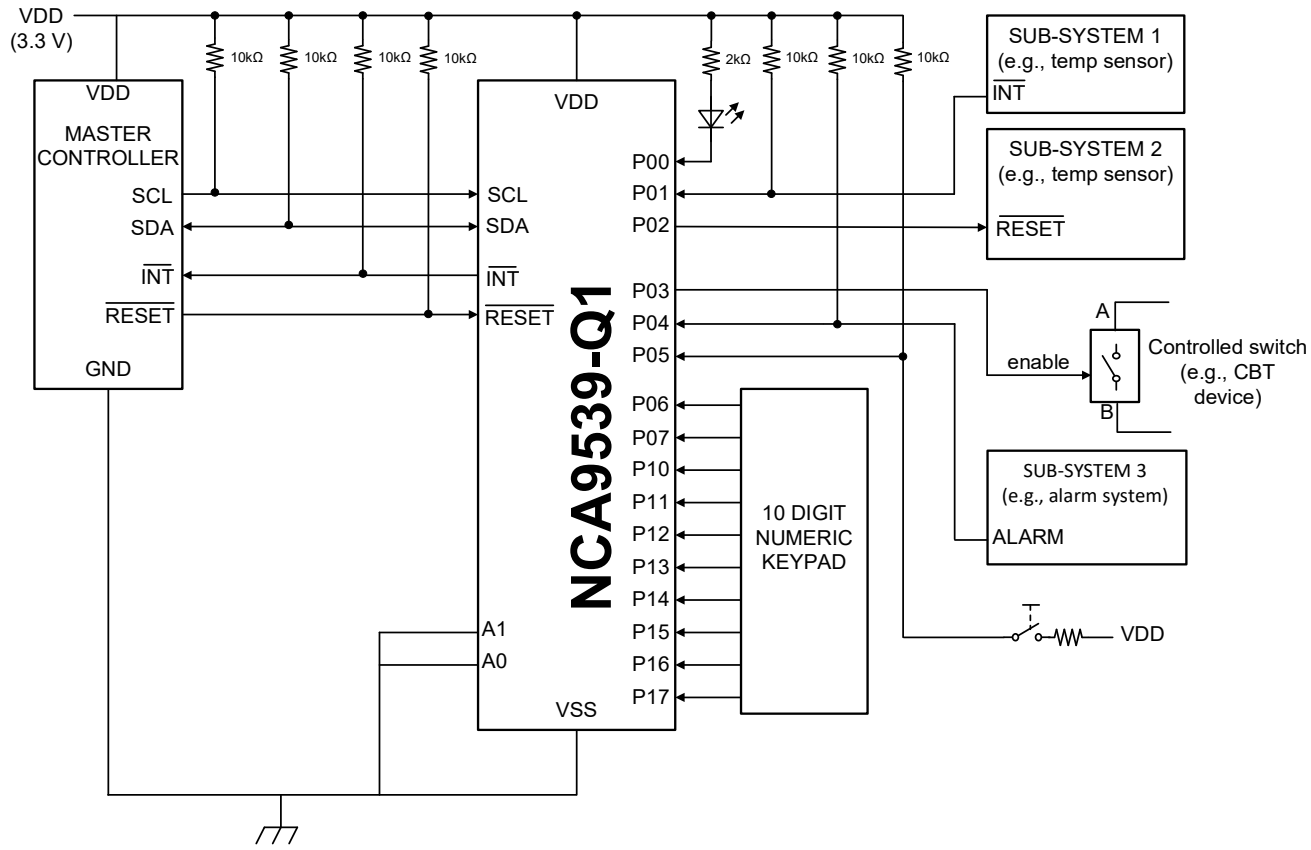


Figure 8-1. Typical Application

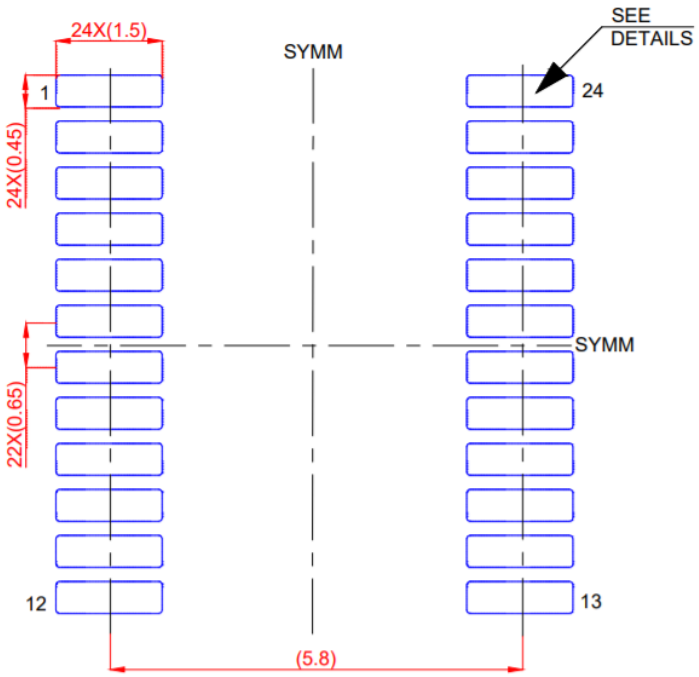
9. Order Information

Part No.	*Temperature*	*MSL Level*	*Package Type*	*Package Drawing*	*Package Qty*
NCA9539-Q1TSXR	-40 to 125°C	1	TSSOP24	TSSOP24	2500
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.					

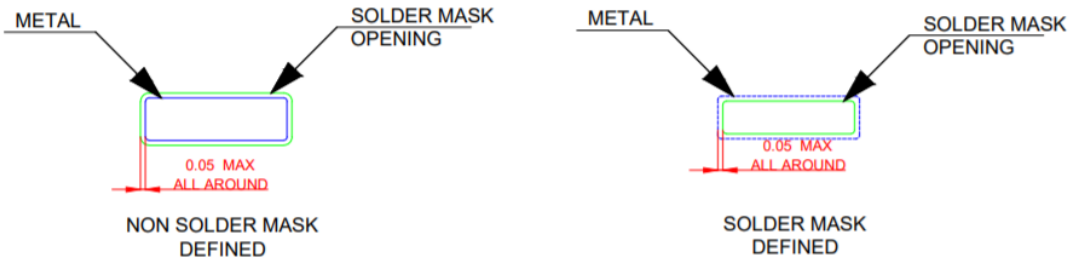
10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NCA9539-Q1	Click here	Click here	Click here

11. Package Information

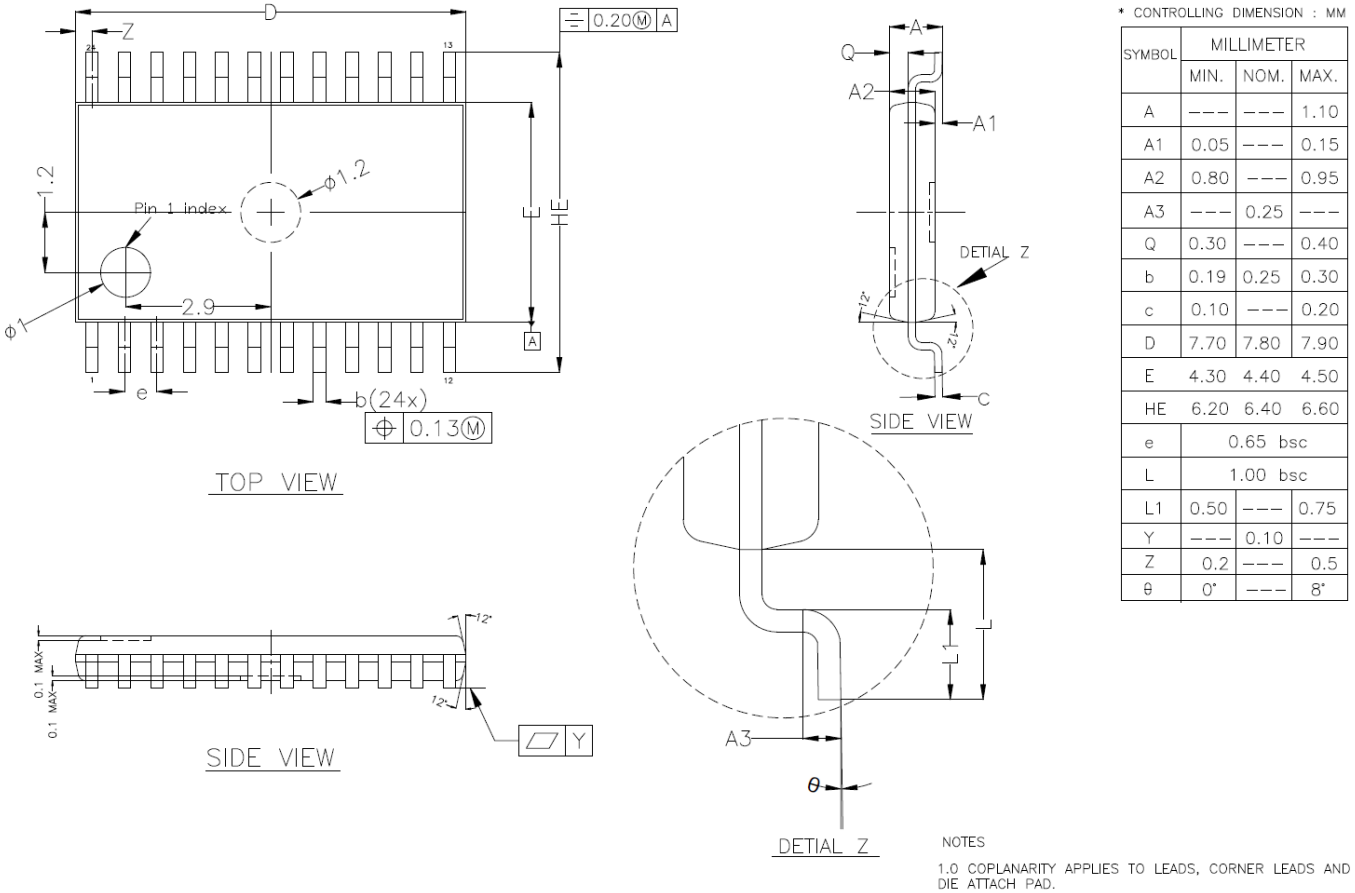


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 11-1. TSSOP24 Footprint Shape and Dimension in millimeters



* CONTROLLING DIMENSION : MM

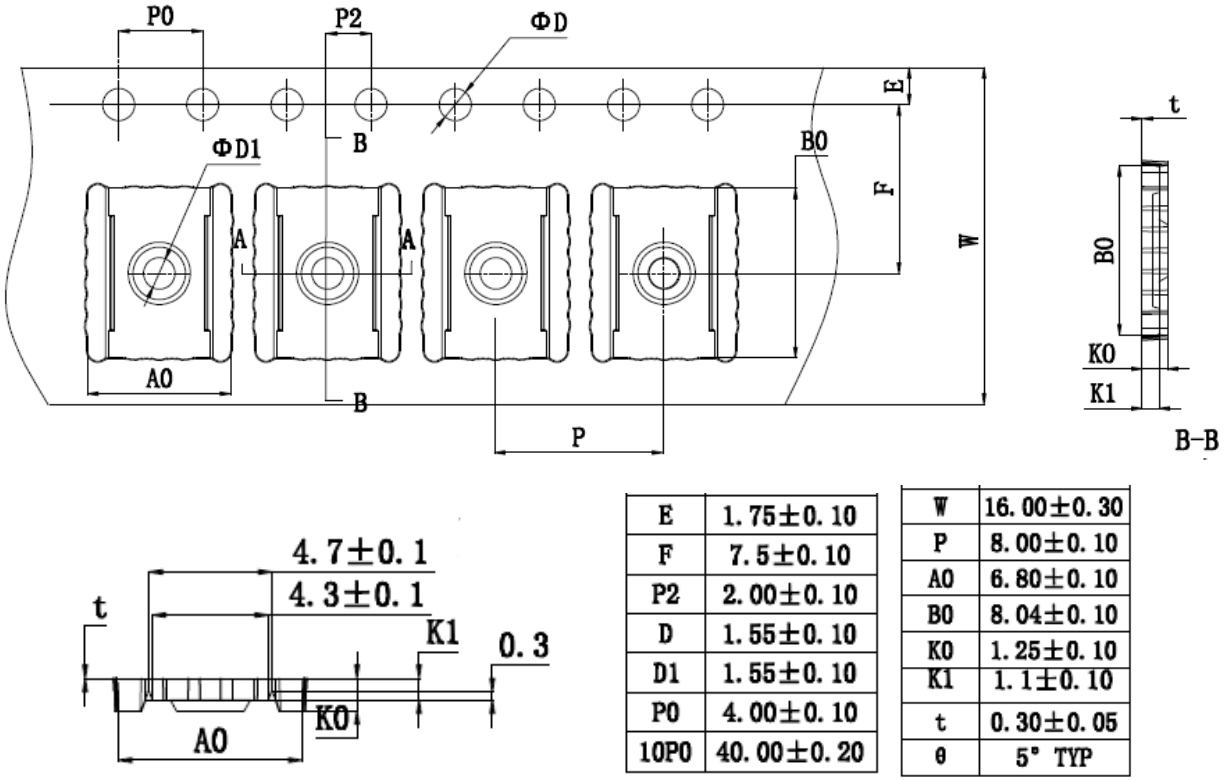
SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	---	0.15
A2	0.80	---	0.95
A3	---	0.25	---
Q	0.30	---	0.40
b	0.19	0.25	0.30
c	0.10	---	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
HE	6.20	6.40	6.60
e	0.65 bsc		
L	1.00 bsc		
L1	0.50	---	0.75
Y	---	0.10	---
Z	0.2	---	0.5
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 11-2. TSSOP24 Package Shape and Dimension in millimeters

12. Tape and Reel Information



E	1.75±0.10
F	7.5±0.10
P2	2.00±0.10
D	1.55±0.10
D1	1.55±0.10
P0	4.00±0.10
10P0	40.00±0.20

W	16.00±0.30
P	8.00±0.10
A0	6.80±0.10
B0	8.04±0.10
K0	1.25±0.10
K1	1.1±0.10
t	0.30±0.05
θ	5° TYP

NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

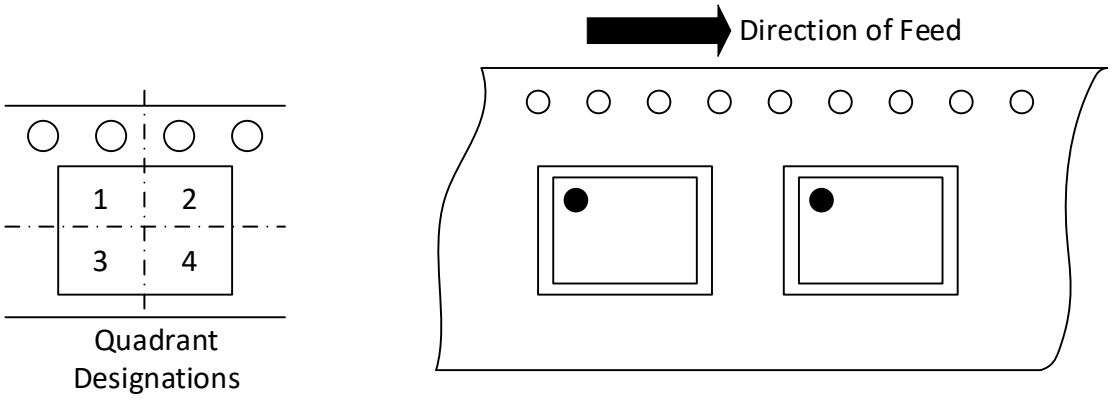


Figure 12-1. Tape and reel information for TSSOP24

13. Revision History

Revision	*Description*	*Date*
1.0	Initial version	2023/1/5
1.1	Added ESD information; figure update; added footprint	2023/10/13
1.2	VDD voltage range expand to 5.5V; simplified schematic update.	2024/5/27

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