NOVOSENSE

# NSOPA905x
# 40-V Rail-to-Rail Input/Output,6MHz, Low Offset Voltage, Low Noise, Operational Amplifier

Datasheet (EN) 1.1

## Product Overview

The NSOPA905x family (NSOPA9051, NSOPA9052, and NSOPA9054) is a family of high voltage (40 V) general purpose operational amplifiers. These devices offer exceptional DC precision and AC performance, including rail-to-rail input/output, low offset (±200 μV, typical), low offset drift (±0.5 μV/°C, typical), low noise (10 nV/√Hz and 4.5 μVPP), and 6MHz bandwidth. Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (60mA), high slew rate (11V/μs), high capacitive load drive (1nF), and shutdown functionality make the NSOPA905x a robust, high performance operational amplifier for high-voltage industrial applications.

The NSOPA905x family of op amps is available in standard packages (SOT-23, MSOP, SOP, and TSSOP), and is specified from -40°C to 125°C.

## Key Features

- Wide supply: ±1.35 V to ±20 V, 2.7 V to 40 V
- Low offset voltage: 200μV typ
- 6MHz GBP
- High slew rate: 11 V/μs typ
- Differential and common-mode input voltage range to supply rail Pulse friendly/comparator inputs
    1. Amplifier operates with differential inputs up to supply rail
    2. Amplifier can be used in open-loop or as comparator
- Low quiescent current: 540 μA per amplifier
- Robust EMIRR performance: EMI/RFI filters on input and supply pins
- RoHS and REACH compliance

## Device Information

| *Part Number* | *Package* | *Body Size* |
|---|---|---|
| NSOPA9051-DSTAR | SOT-23 (5) | 2.90 mm × 1.60 mm |
| NSOPA9051-DSPR | SOP (8) | 4.90 mm × 3.90 mm |
| NSOPA9052-DSPR | SOP (8) | 4.90 mm × 3.90 mm |
| NSOPA9052-DMSR | MSOP (8) | 3.00 mm × 3.00 mm |
| NSOPA9054-DSPKR | SOP (14) | 8.65 mm × 3.9 mm |
| NSOPA9054-DTSKR | TSSOP (14) | 5.00 mm × 4.40 mm |

## Typical Application

- Multiplexed data-acquisition systems
- Test and measurement equipment
- ADC driver amplifiers
- SAR ADC reference buffers
- Programmable logic controllers
- High-side and low-side current sensing

# INDEX

# 1. Pin Configuration and Functions

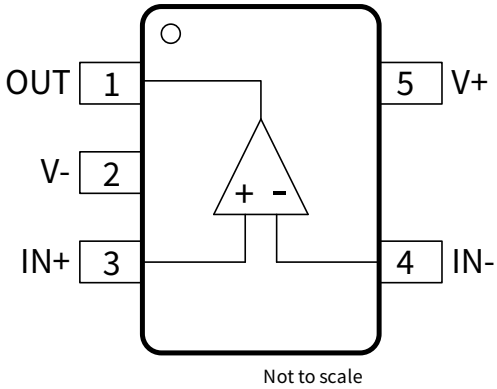



Figure 1-1 NSOPA9051 5-Pin SOT-23 Package Top View

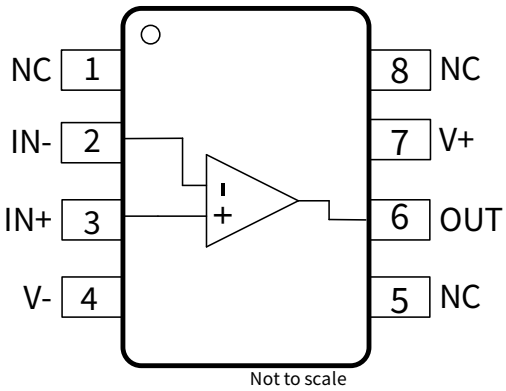



Figure 1-2 NSOPA9051 8-Pin SOP Package Top View

Table 1-1 NSOPA9051 Pin Configuration and Description

| *Symbol* | 5-Pin SOT-23 *No.* | 8-Pin SOP *No.* | *Function* |
|---|---|---|---|
| IN+ | 3 | 3 | Noninverting Input |
| IN- | 4 | 2 | Inverting Input |
| OUT | 1 | 6 | Output |
| V+ | 5 | 7 | Positive Power supply |
| V- | 2 | 4 | Negative Power supply |
| NC | - | 1 | Do not connect |
| NC | - | 5 | Do not connect |
| NC | - | 8 | Do not connect |

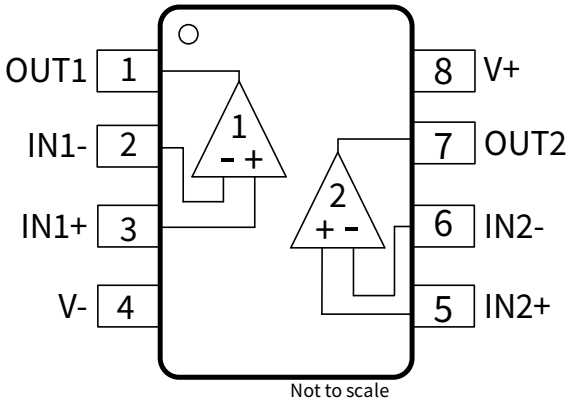



Figure 1-3 NSOPA9052 8-Pin SOP and MSOP Package Top View

Table 1-2 NSOPA9052 Pin Configuration and Description

| *Symbol* | *No.* | *Function* |
|---|---|---|
| IN1- | 2 | Channel 1 Inverting Input |
| IN1+ | 3 | Channel 1 Noninverting Input |
| OUT1 | 1 | Channel 1 Output |
| IN2- | 6 | Channel 2 Inverting Input |
| IN2+ | 5 | Channel 2 Noninverting Input |
| OUT2 | 7 | Channel 2 Output |
| V+ | 8 | Positive Power Supply |
| V- | 4 | Negative Power Supply |

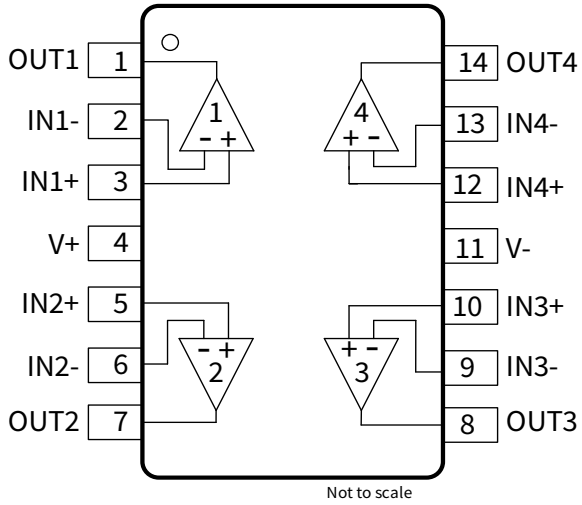



Figure 1-4 NSOPA9054 14-Pin SOP and TSSOP Package Top View

Table 1-3 NSOPA9054 Pin Configuration and Description

| *Symbol* | *No.* | *Function* |
|---|---|---|
| IN1- | 2 | Channel 1 Inverting Input |
| IN1+ | 3 | Channel 1 Noninverting Input |
| OUT1 | 1 | Channel 1 Output |
| IN2– | 6 | Channel 2 Inverting Input |
| IN2+ | 5 | Channel 2 Noninverting Input |
| OUT2 | 7 | Channel 2 Output |
| IN3– | 9 | Channel 3 Inverting Input |
| IN3+ | 10 | Channel 3 Noninverting Input |
| OUT3 | 8 | Channel 3 Output |
| IN4– | 13 | Channel 4 Inverting Input |
| IN4+ | 12 | Channel 4 Noninverting Input |
| OUT4 | 14 | Channel 4 Output |
| V+ | 4 | Positive Power Supply |
| V- | 11 | Negative Power Supply |

## 2. Absolute Maximum Ratings[1]

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage $V_S = (V_+) - (V_-)$ | $V_S$ | -0.3 | 42 | V |
| Differential, IN+ to IN− inputs | | | $(V_+)+0.5$ | V |
| Common-Mode input voltage | | $(V_-)-0.5$ | $(V_+)+0.5$ | V |
| Output | | $(V_-)-0.5$ | $(V_+)+0.5$ | V |
| Junction temperature | $T_J$ | | 150 | °C |
| Storage temperature | $T_{stg}$ | −55 | 150 | °C |

## 3. ESD Ratings

| Parameters | Ratings | Value | Unit |
|---|---|---|---|
| Electrostatic discharge | ● Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 | ±2000 | V |
| | ● Charged device model (CDM), per JEDEC specification JESD22-C101 | ±2000 | V |

## 4. Recommended Operating Conditions

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_S$ | 2.7 | 40 | V |
| Operating free-air temperature | $T_A$ | -40 | 125 | °C |

## 5. Thermal Information

| Parameters | Symbol | SOT23-5L | SOP-8 | MSOP-8 | TSSOP-14 | SOP-14 | Unit |
|---|---|---|---|---|---|---|---|
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 185.7 | 130.7 | 176.5 | 131.4 | 101.4 | °C/W |
| Junction-to-case (top) thermal resistance | $\theta_{JC}$ | 108.2 | 72.8 | 68.1 | 51.8 | 57.6 | °C/W |
| Junction-to-board thermal resistance | $\theta_{JB}$ | 54.5 | 74.0 | 98.2 | 75.8 | 57.3 | °C/W |
| Junction-to-top characterization parameter | $\Psi_{JT}$ | 31.2 | 24.0 | 12.0 | 7.9 | 18.5 | °C/W |
| Junction-to-board characterization parameter | $\Psi_{JB}$ | 54.2 | 73.3 | 96.7 | 74.8 | 56.9 | °C/W |

[1] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

# 6. Electrical Characteristics

$V_S$ = ($V_+$) – ($V_-$) = 40 V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S$/2, $V_{CM}$ = $V_S$/2, and $V_{OUT}$ = $V_S$/2, unless otherwise noted.

| Parameters | Symbol | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| Offset voltage | $V_{OS}$ | $V_{CM}$ = ($V_-$) | | | ±0.2 | ±1.2 | mV |
| | | $T_A$ =–40°C to 125°C[1] | | | | ±1.55 | |
| Offset voltage drift | $dV_{OS}/dT$ | $T_A$ =–40°C to 125°C[1] | | | ±0.5 | | µV/°C |
| Common-mode input range | $V_{CM}$ | | | ($V_-$)-0.1 | | ($V_+$)+0.1 | V |
| Common mode rejection ratio | CMRR | $V_S$ = 40V, ($V_-$)–0.1V < $V_{CM}$ < ($V_+$)–2.5V (PMOS pair) | $T_A$ =25°C | 107 | 123 | | dB |
| | | | $T_A$ =–40°C to 125°C[1] | 102 | | | |
| | | $V_S$ = 4V, ($V_-$)–0.1V < $V_{CM}$ < ($V_+$)–2.5V (PMOS pair) | $T_A$ =25°C | 81 | 96 | | |
| | | | $T_A$ =–40°C to 125°C[1] | 76 | | | |
| | | $V_S$ = 2.7V, ($V_-$)–0.1V < $V_{CM}$ < ($V_+$)–2.5V (PMOS pair) | $T_A$ =25°C | 72 | 85 | | |
| | | | $T_A$ =–40°C to 125°C[1] | 69 | | | |
| Channel Separation | | f =0Hz | | | 120 | | dB |
| Input bias current | $I_B$ | $V_S$ = 2.7V to 40V, $V_{CM}$ = $V_S$/2 | | | ±15 | | pA |
| | | $T_A$ =–40°C to 125°C[1] | | | ±20 | | nA |
| Input offset current | $I_{OS}$ | $V_S$ = 2.7V to 40V, $V_{CM}$ = $V_S$/2 | | | ±5 | | pA |
| | | $T_A$ =–40°C to 125°C[1] | | | ±10 | | nA |
| Input Impedance | $Z_{ID}$ | Differential | | | 1.9\|\|5 | | GΩ\|\|pF |
| | $Z_{ICM}$ | Common-mode | | | 0.2\|\|4 | | TΩ\|\|pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| Open-loop voltage gain | $A_{OL}$ | $V_S$ = 40V, No load, ($V_-$)+0.2V<$V_O$<($V_+$)–0.2V | $T_A$ =25°C | 129 | 145 | | dB |
| | | | $T_A$ =–40°C to 125°C[1] | | 126 | | |
| | | $V_S$ = 4V, No load, ($V_-$) +0.2V<$V_O$<($V_+$)–0.2V | $T_A$ =25°C | 110 | 125 | | |
| | | | $T_A$ =–40°C to 125°C[1] | | 115 | | |
| | | $V_S$ = 2.7V, No load, ($V_-$) +0.2V<$V_O$<($V_+$)–0.2V | $T_A$ =25°C | 107 | 123 | | |
| | | | $T_A$ =–40°C to 125°C[1] | | 112 | | |

[1] Data under $T_A$=–40°C to 125°C condition is guaranteed by Characterization only.

## Electrical Characteristics (continued)

$V_S$ = ($V_+$) – ($V_-$) = 40 V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S$/2, $V_{CM}$ = $V_S$/2, and $V_{OUT}$ = $V_S$/2, unless otherwise noted.

| Parameters | Symbol | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| Output swing from rail headroom | | $V_S$=2.7~40V, $R_L$=no load | | | 1 | 5 | mV |
| | | $V_S$=2.7V, $R_L$=10kΩ | | | 5 | 10 | |
| | | $V_S$=40V, $R_L$=10kΩ | | | 50 | 55 | |
| | | $V_S$=2.7V, $R_L$=2kΩ | | | 22 | 40 | |
| | | $V_S$=40V, $R_L$=2kΩ | | | 230 | 265 | |
| Short-circuit current | $I_{SC}$ | Sinking | | | 60 | | mA |
| | | Sourcing | | | 85 | | |
| Output impedance | $Z_O$ | f = 1 MHz, $I_O$ = 0 A | | | 200 | | Ω |
| **FREQUENCY RESPONSE** | | | | | | | |
| Gain-bandwidth product | GBP | $V_S$ = 40 V, $C_L$ = 10 pF | | | 6 | | MHz |
| Phase margin | PM | $V_S$ = 40 V, $C_L$ = 10 pF | | | 52 | | Degree |
| Settling time | $T_S$ | To 0.1%, 10 V Step, $C_L$ = 10 pF | | | 1.7 | | µs |
| | | To 0.1%, 2 V Step, $C_L$ = 10 pF | | | 0.8 | | |
| | | To 0.01%, 10 V Step, $C_L$ = 10 pF | | | 2 | | |
| | | To 0.01%, 2 V Step, $C_L$ = 10 pF | | | 1.5 | | |
| Slew rate | Rising | 10-V step, G= +1 | | | 14 | | V/µs |
| | Falling | | | | 11 | | |
| Total harmonic distortion + noise | THD+N | $V_{rms}$ = 1 V, G = 1, f = 1 kHz, $R_L$= 10kΩ | | | 110 | | dB |
| Overload recovery time | | $V_{IN}$ × Gain > $V_S$ | | | 400 | | ns |
| EMI rejection ratio | EMIRR | f = 1GHz | | | 80 | | dB |
| **NOISE (INPUT REFERRED)** | | | | | | | |
| Input voltage noise density | $e_n$ | f = 1 kHz | | | 19 | | nV/$\sqrt{Hz}$ |
| | | f = 10 kHz | | | 10 | | |
| Input voltage noise | $e_{n\ p\text{-}p}$ | f = 0.1 Hz to 10 Hz | | | 4.5 | | µVpp |
| **POWER SUPPLY** | | | | | | | |
| Operating voltage range | $V_S$ | | | 2.7 | | 40 | V |
| Power supply rejection ratio | PSRR | $V_S$ = 4V to 40V, $V_{CM}$ = ($V_-$) | $T_A$ =25°C | 124 | 140 | | dB |
| | | | $T_A$ =–40°C to 125°C[1] | 117 | | | |
| | | $V_S$ = 2.7V to 40V, $V_{CM}$ = ($V_-$) | $T_A$ =25°C | 110 | 125 | | |
| | | | $T_A$ =–40°C to 125°C[1] | 104 | | | |
| Quiescent current | $I_Q$ | $V_S$=2.7V | | | 500 | 650 | µA |
| | | $V_S$=2.7V, $T_A$ =–40°C to 125°C[1] | | | | 830 | |
| | | $V_S$=40V | | | 540 | 705 | |
| | | $V_S$=40V, $T_A$ =–40°C to 125°C[1] | | | | 880 | |

[1] Data under $T_A$=–40°C to 125°C condition is guaranteed by Characterization only.

# 7. Typical Performance Characteristics

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

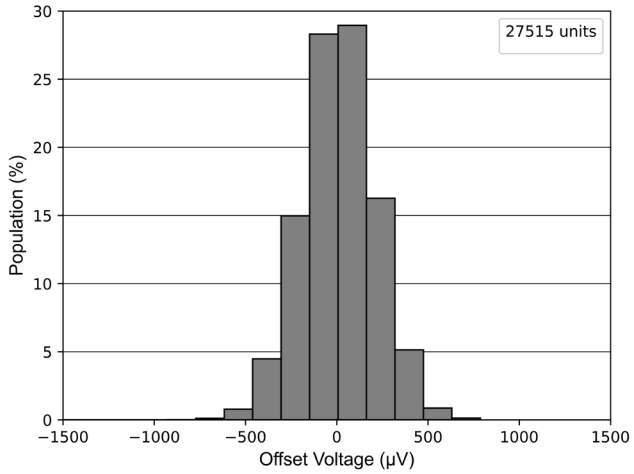



Figure 7-1 Offset Voltage Production Distribution ($V_{CM} = V_-$)

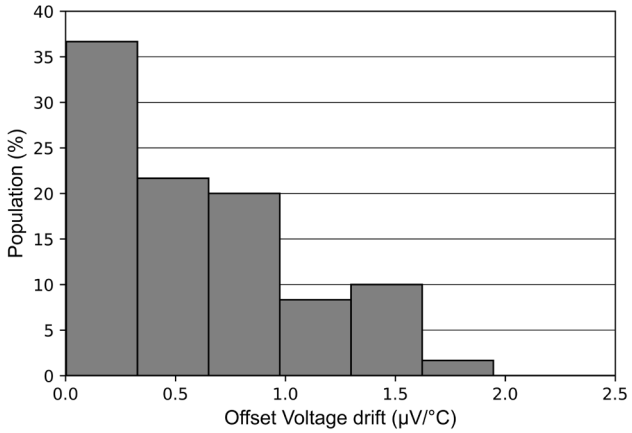



Figure 7-2 Offset Voltage Drift Distribution ($V_{CM} = V_-$)

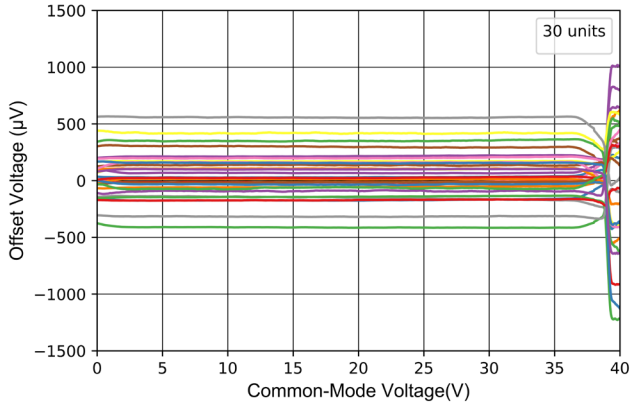



Figure 7-3 Offset Voltage vs Common-Mode Voltage

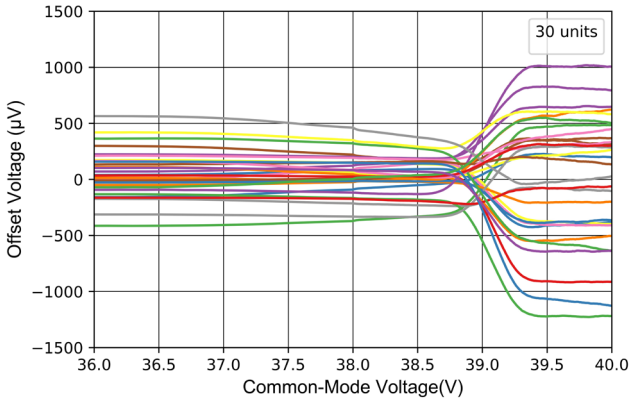



Figure 7-4 Offset Voltage vs Common-Mode Voltage (Transition Area)

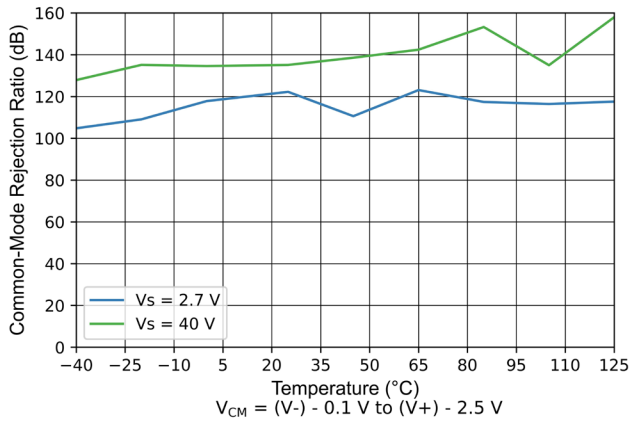



Figure 7-5 CMRR vs Temperature

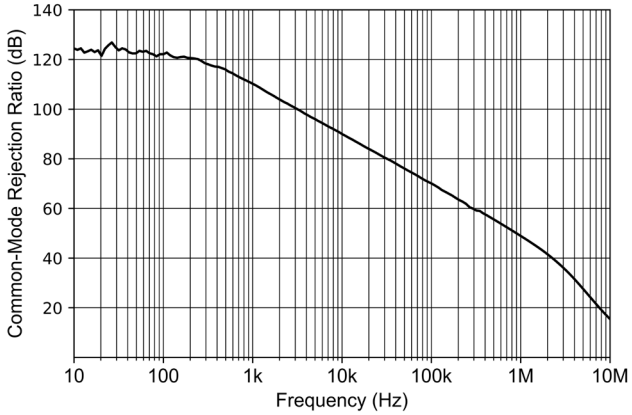



Figure 7-6 Common-Mode Rejection Ratio vs Frequency

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

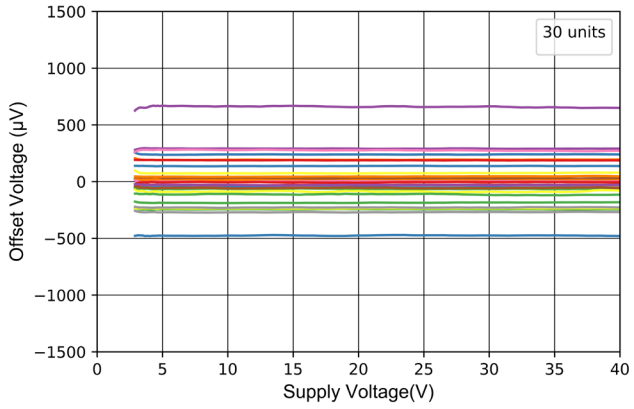



Figure 7-7 Offset Voltage vs Power Supply ($V_{CM} = V_-$)

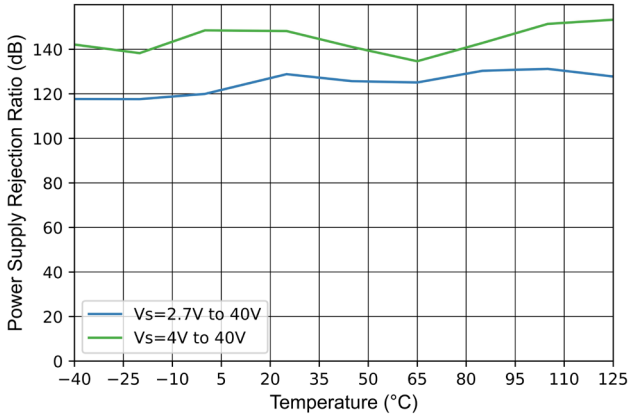



Figure 7-8 PSRR vs Temperature

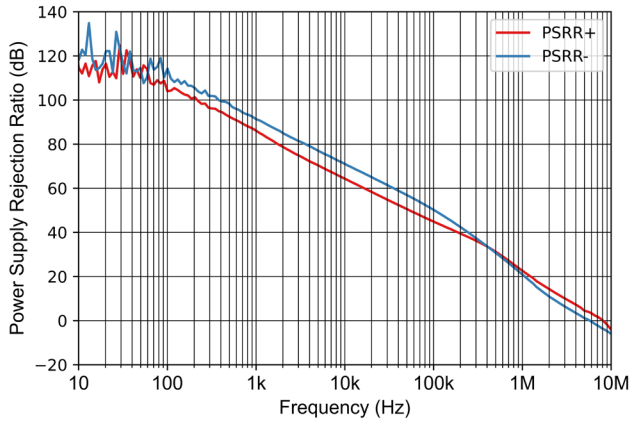



Figure 7-9 Power-Supply Rejection Ratio vs Frequency

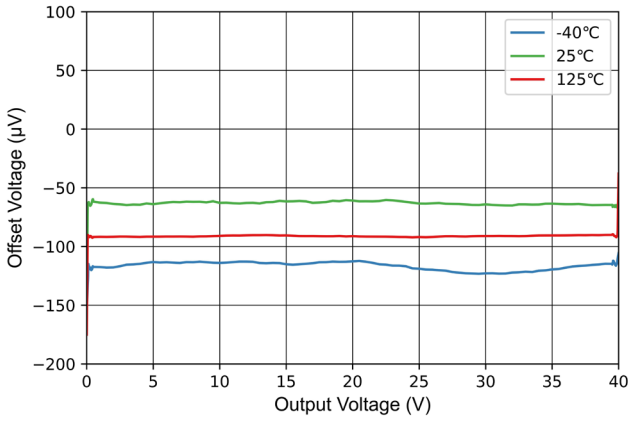



Figure 7-10 Offset Voltage vs Output Voltage

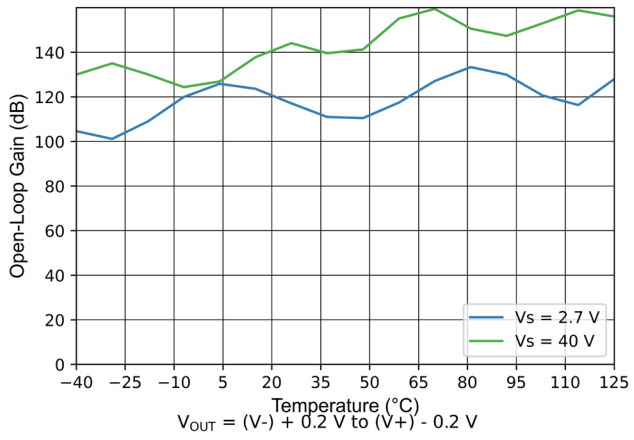



Figure 7-11 Open-Loop Voltage Gain vs Temperature

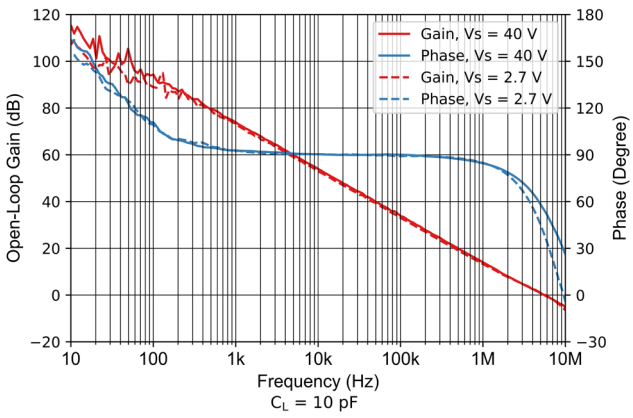



Figure 7-12 Open Loop Gain vs Frequency

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

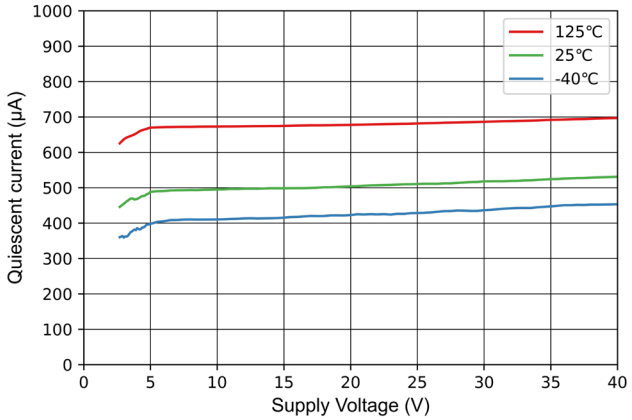



Figure 7-13 Quiescent Current vs Supply Voltage ($V_{CM} = V_-$)

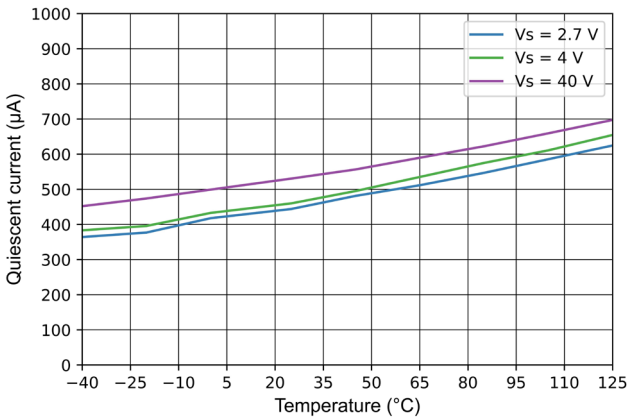



Figure 7-14 Quiescent Current vs Temperature

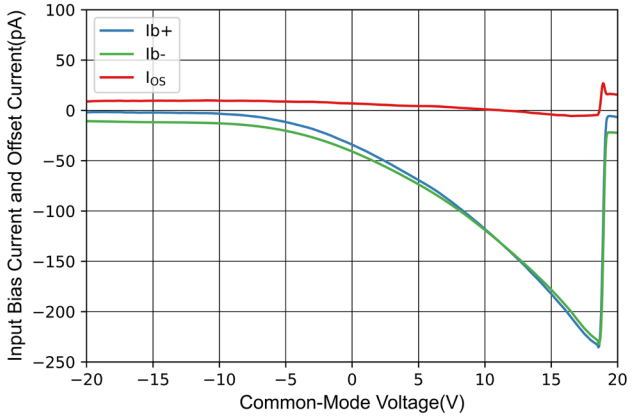



Figure 7-15 Input Bias Current vs Common-Mode Voltage

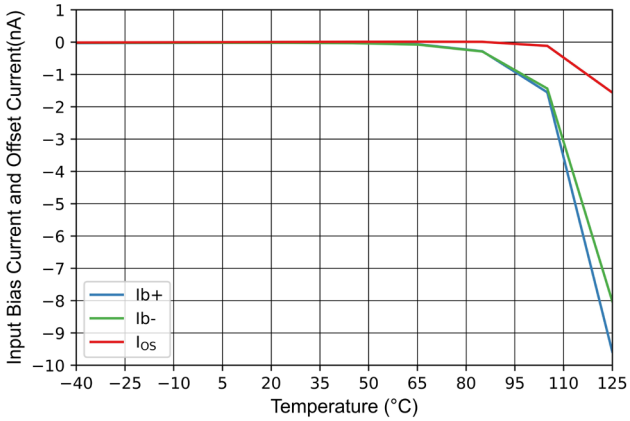



Figure 7-16 Input Bias Current vs Temperature

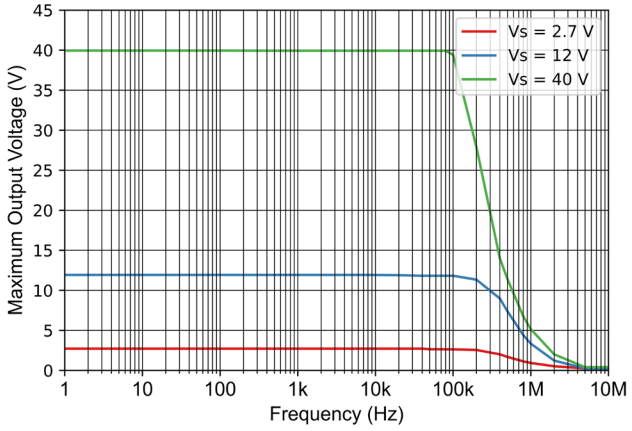



Figure 7-17 Maximum Peak Output Voltage vs. Frequency

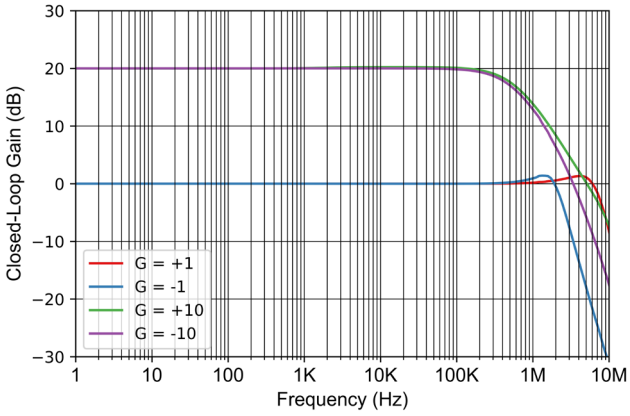



Figure 7-18 Closed Loop Gain and Phase vs Frequency

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

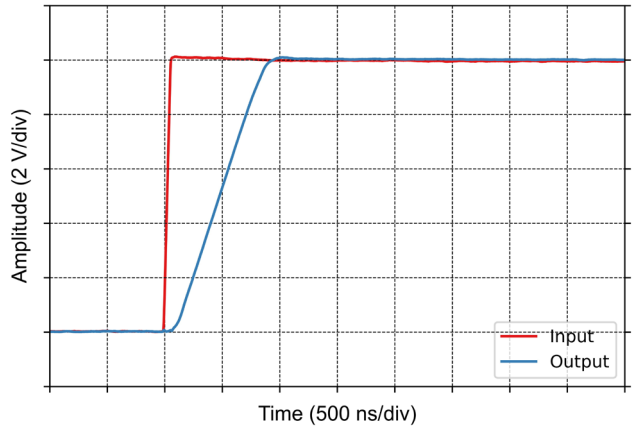



Figure 7-19 Large-Signal Step Response (Rising)

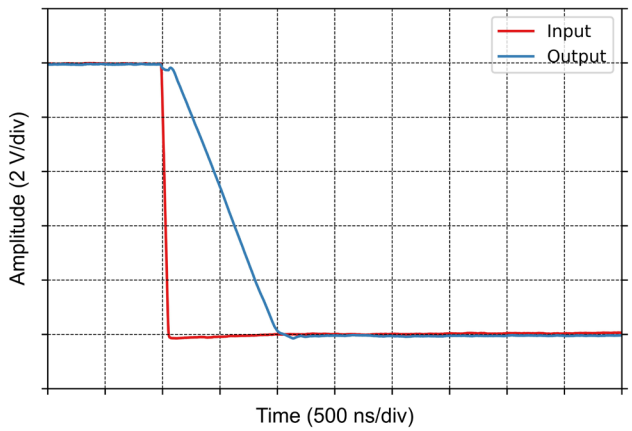



Figure 7-20 Large-Signal Step Response (Falling)

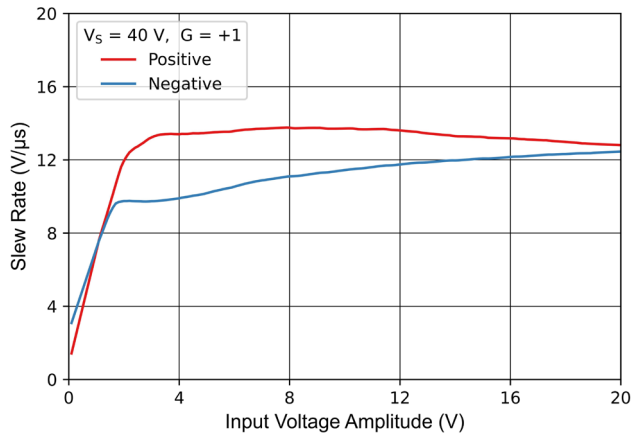



Figure 7-21 Slew Rate vs Input Voltage Amplitude

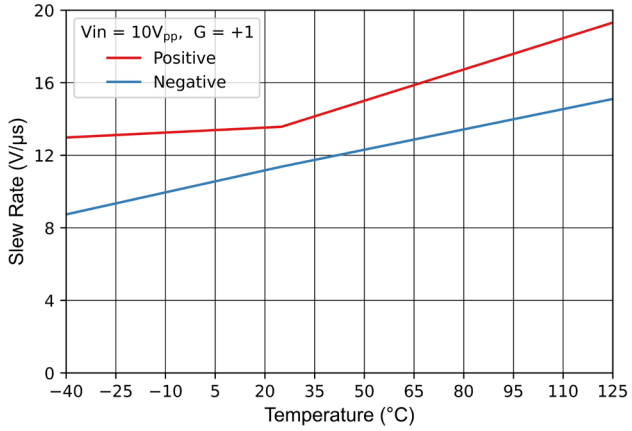



Figure 7-22 Slew Rate vs Temperature

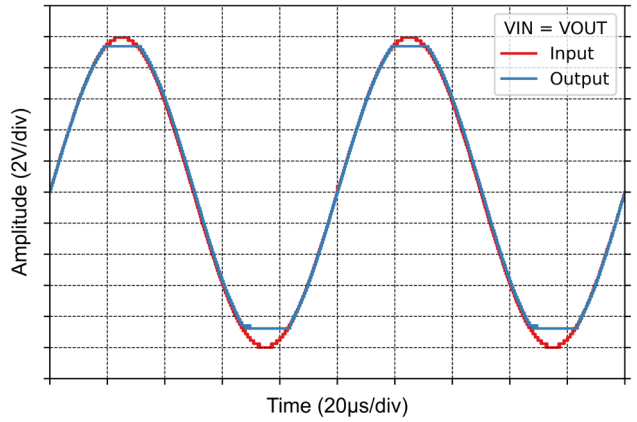



Figure 7-23 No Phase Reversal

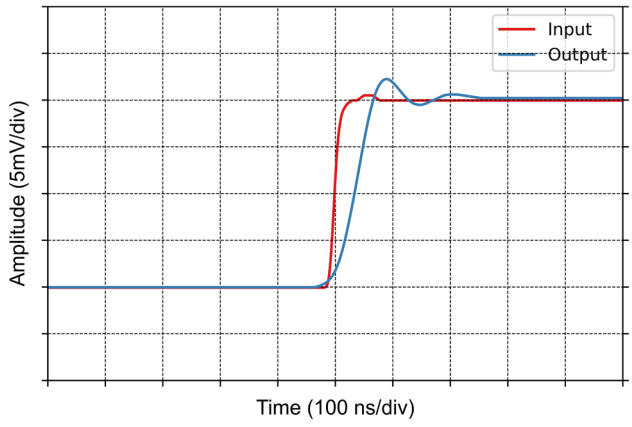



Figure 7-24 Small-Signal Step Response

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

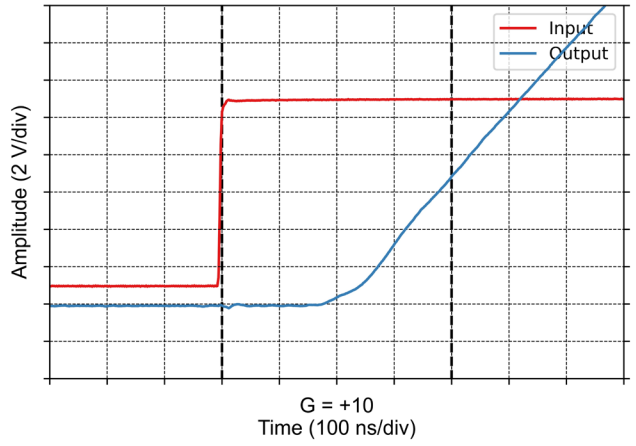



Figure 7-25 Positive Overload Recovery

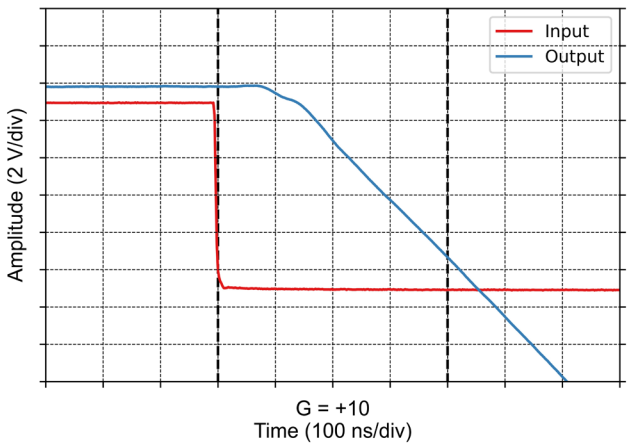



Figure 7-26 Negative Overload Recovery

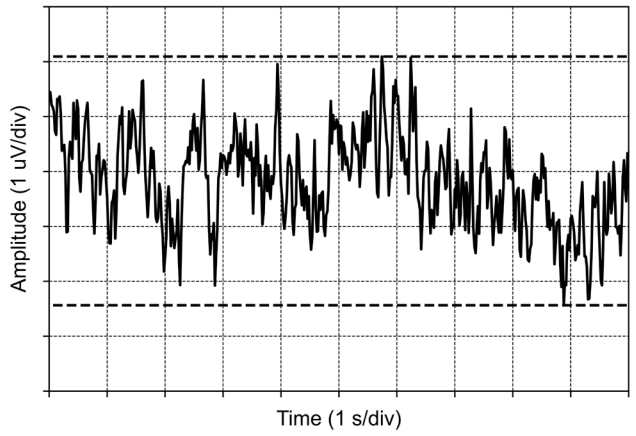



Figure 7-27 0.1-Hz to 10-Hz Noise

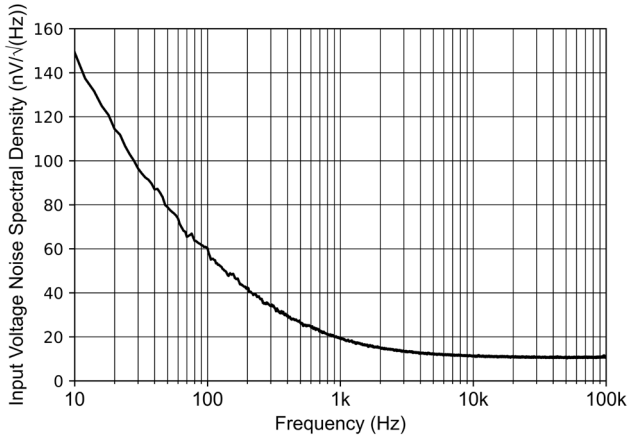



Figure 7-28 Input Voltage Noise Spectral Density

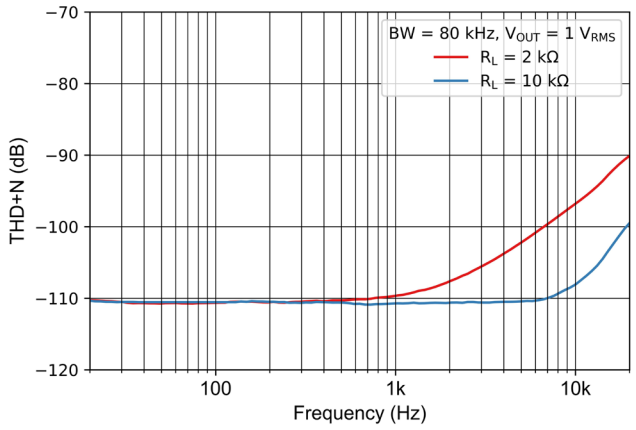



Figure 7-29 THD+N Ratio vs Frequency

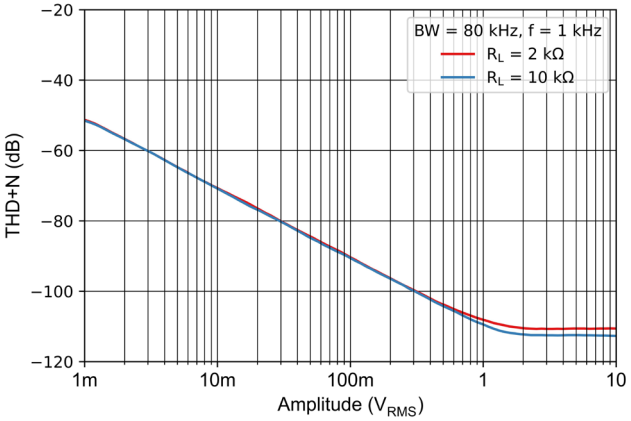



Figure 7-30 THD+N vs Output Amplitude

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

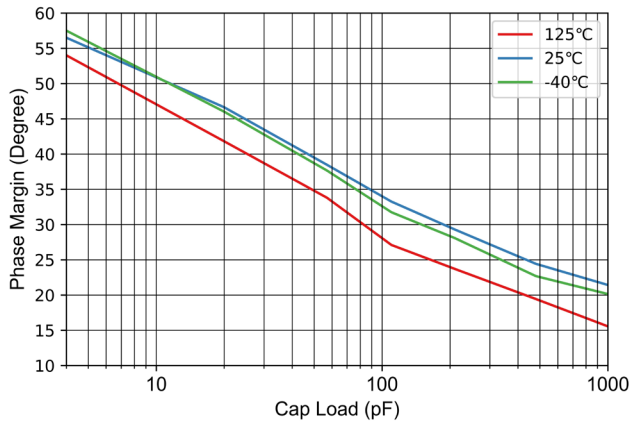



Figure 7-31 Phase Margin vs Capacitive Load

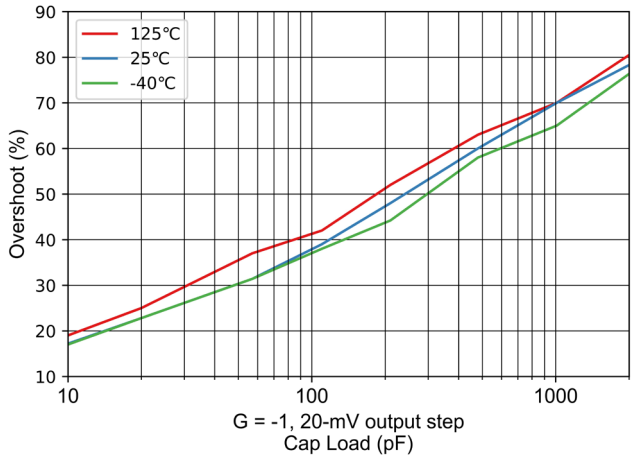



Figure 7-32 Small-Signal Overshoot vs Capacitive Load

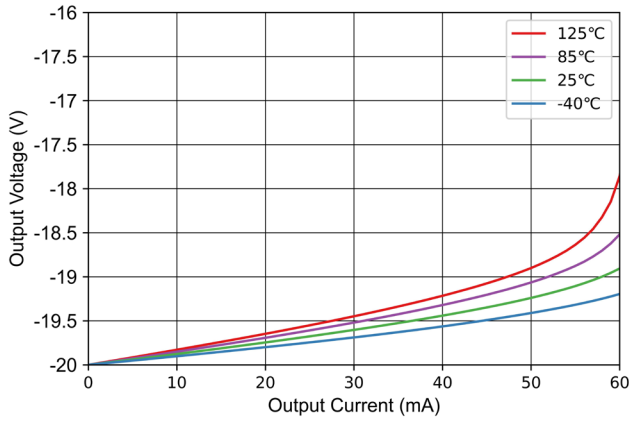



Figure 7-33 Output Voltage Swing vs Output Sinking Current

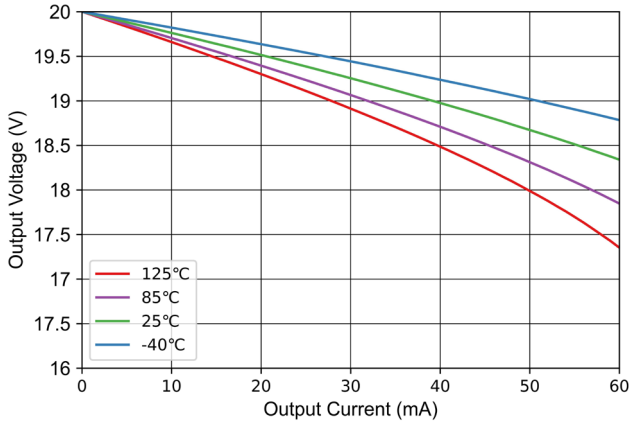



Figure 7-34 Output Voltage Swing vs Output Sourcing Current

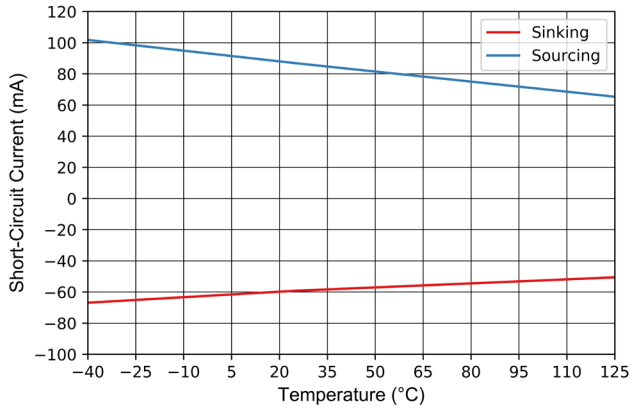



Figure 7-35 Short-Circuit vs Temperature

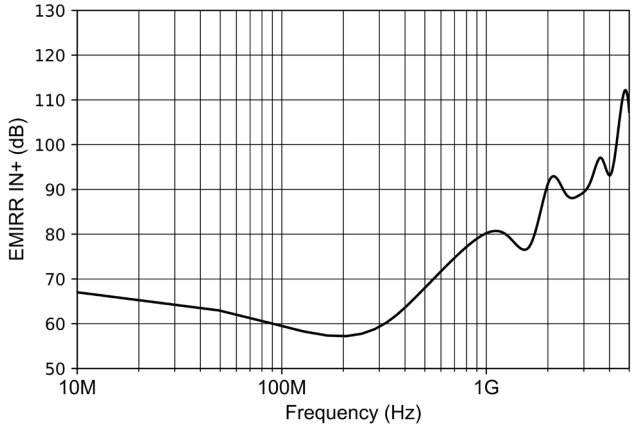



Figure 7-36 EMIRR vs Frequency

## Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 40$ V (±20 V) at $T_A$ =25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

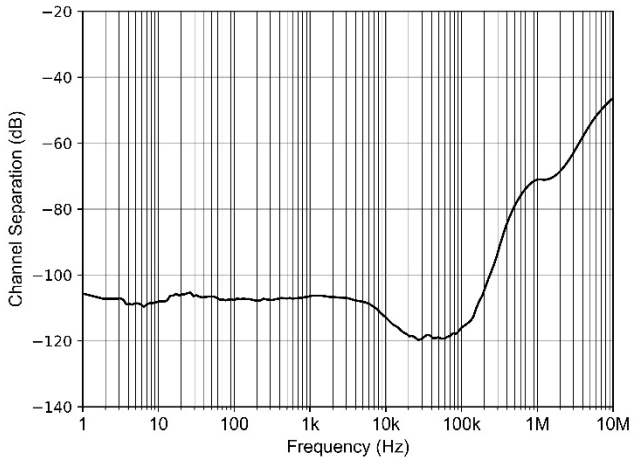



Figure 7-37 Channel Separation vs Frequency

# 8. Function Description

## 8.1. Overview

The NSOPA905x series are high-voltage general-purpose amplifiers that can operate up to 40V. These devices offer excellent parameters and are particularly suitable for high slew rate and cost-sensitive applications that will require high voltage signals, such as motor drives and inverter systems.

## 8.2. Functional Block Diagram

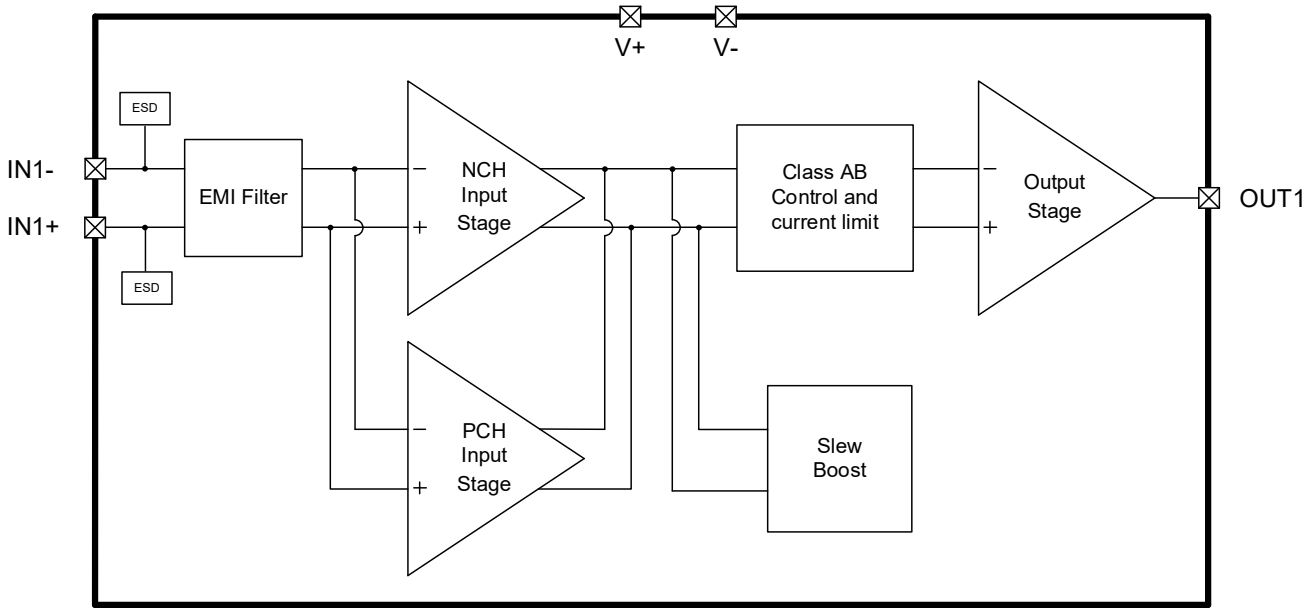



Figure 8-1 NSOPA905x Functional block Diagram (One channel is shown)

## 8.3. Feature Description

### 8.3.1. Pulse Friendly

Traditional op amps use back-to-back diode input stages to limit the differential input range. If the device operates in open-loop conditions, once the voltage between the two input pins exceeds the limit voltage, unexpected current will flow into the device and may cause device damage.

Using new input stage topology, NSOPA905x provides full 40v differential input range. when it works in open-loop case, it will not sink any current from source and behave as the comparator.

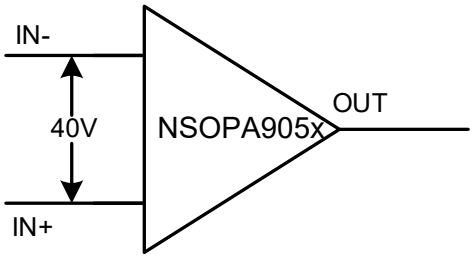



Figure 8-2 NSOPA905x input stage

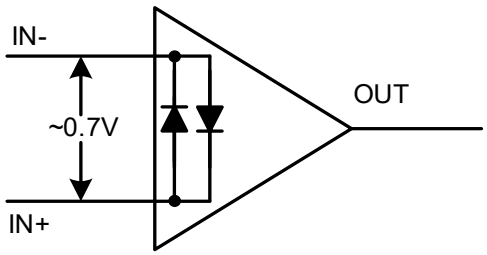



Figure 8-3 Traditional op-amp input stage

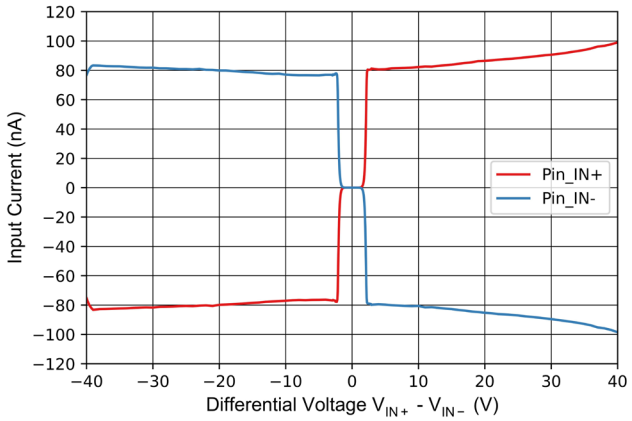



Figure 8-4 Input Current vs Input Differential Voltage, open-loop

### 8.3.2. Slew Rate Boost

Because of slew rate boost feature, document state that NSOPA905X has a about 11V/μs slew rate. Actually, the slew rate of device depends on the input amplitude voltage. The figure illustrates the behavior of this feature.

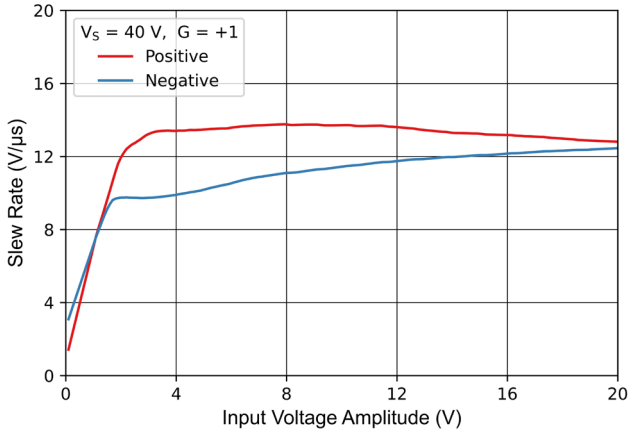



Figure 8-5 Slew-Rate vs Input Voltage Amplitude

### 8.3.3. Common-Mode Input Stage

The NSOPA905x is a 40V true rail-to-rail input op amp with an input common-mode range of 100mV beyond either supply rail. This wide range is achieved by paralleling complementary N-channel and P-channel differential input pairs, as shown in Figure *8-6*. N-channel pairs are active when the input voltage is close to the positive supply rail, typically – 1 V to 100 mV above the positive supply (V+). The P-channel pair is active over an input range from 100 mV below the negative supply to approximately (V+) – 2.5 V. There is a small transition region, typically (V+) – 2.5 V to (V+) – 1 V, where both input pairs are on. This transition region will vary slightly with process variations, and within this region, PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

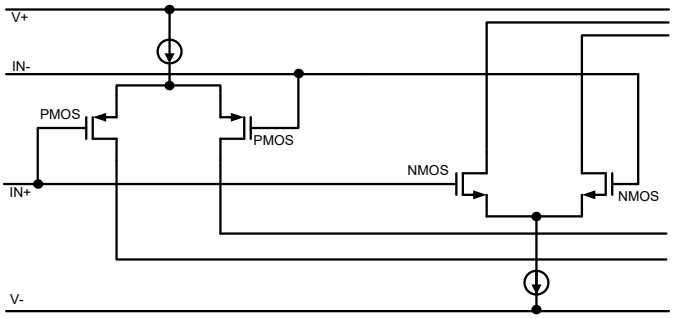



Figure 8-6 NSOPA905x Rail-to-rail Input Stage

### 8.3.4. EMI Rejection

The NSOPA905x uses integrated electromagnetic interference (EMI) filtering to reduce the impact of EMI from sources such as wireless communications and densely populated circuit boards that mix analog signal chains and digital components. The advantage of NSOPA905x is that EMI immunity can be improved through circuit design technology. Figure 8-7 shows the test results on NSOPA905x.

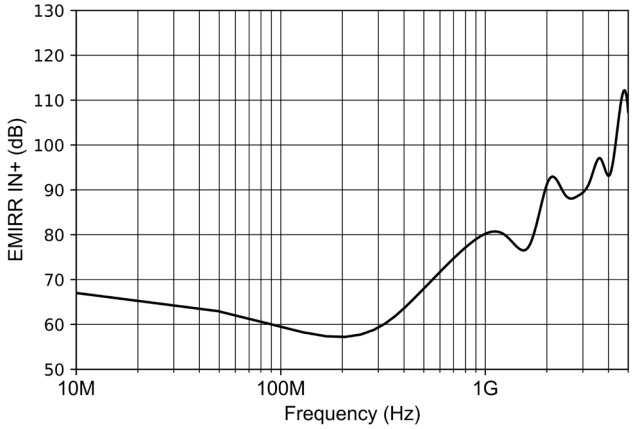



Figure 8-7 NSOPA905x EMIRR vs Frequency

### 8.3.5. Drive Capacitive Load

The NSOPA905x has a resistive output stage capable of driving moderate capacitive loads, and by utilizing isolation resistors, the device can be easily configured to drive large capacitive loads. The specific op amp circuit configuration, layout, gain, and output loading are important factors in determining whether the amplifier will operate stably Some factors to consider.

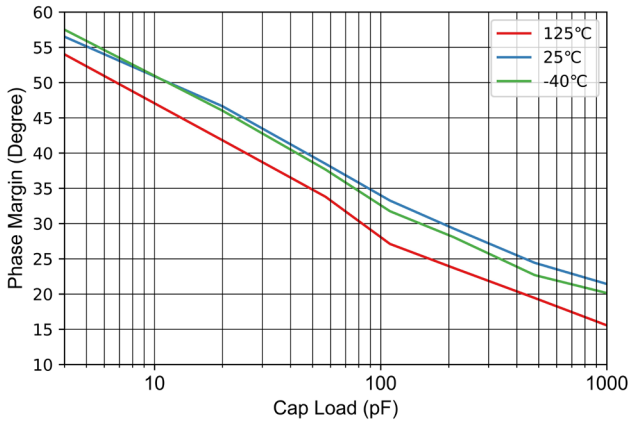



Figure 8-8 NSOPA905x Phase Margin vs Capacitive Load

To obtain additional drive capability in a unity-gain configuration, capacitive load drive can be improved by inserting a small resistor, $R_{ISO}$, in series with the output, as shown in Figure 8-9. This resistor significantly reduces ringing and maintains DC performance under purely capacitive loads. However, if a resistive load is placed in parallel with a capacitive load, a voltage divider is created, which introduces a gain error at the output and slightly reduces the output swing. The error introduced is proportional to the ratio $R_{ISO}/R_L$ and is usually negligible at low voltage output levels.

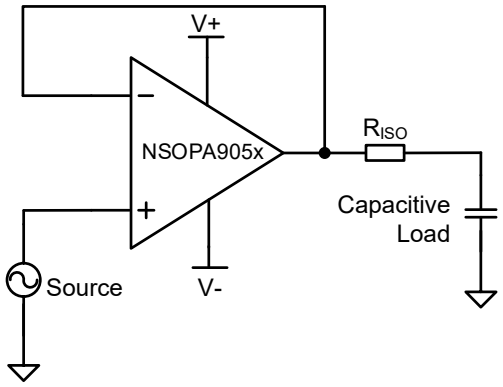



Figure 8-9 Insert isolation Resistor to drive large Capacitive Load

### 8.3.6. Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called self-heating. The absolute maximum junction temperature of the NSOPA905x is 150°C.

Exceeding this temperature may damage the device. The NSOPA905x features thermal protection to reduce damage caused by self-heating. This protection is achieved by monitoring the device temperature and turning off the op amp output drive when the temperature is above 170°C. Figure 8-10 shows an application example of nsopa905x that has significant self-heating due to power dissipation (0.5 W). Thermal calculations show that for an ambient temperature of 105°C, the device junction temperature must reach 177°C. However, real devices shut down the output drive to return to a safe junction temperature. Figure 8-10 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 10V. When self-heating causes the device junction temperature to rise above internal limits, thermal protection forces the output into a high-impedance state and pulls the output to ground through resistor RL.

If the condition causing excessive power dissipation is not removed, the amplifier will remain in an off and enabled state until the output fault is corrected.

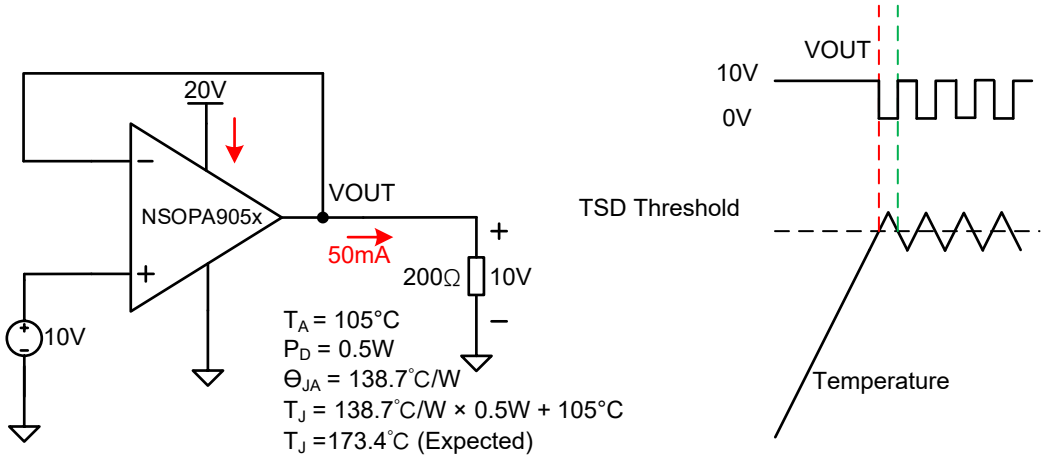



Figure 8-10 Thermal shut down and recovery

### 8.3.7. Electrical Overstress

Always, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-11 shows an illustration of the ESD circuits contained in the NSOPA905x (indicated by the dotted area area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

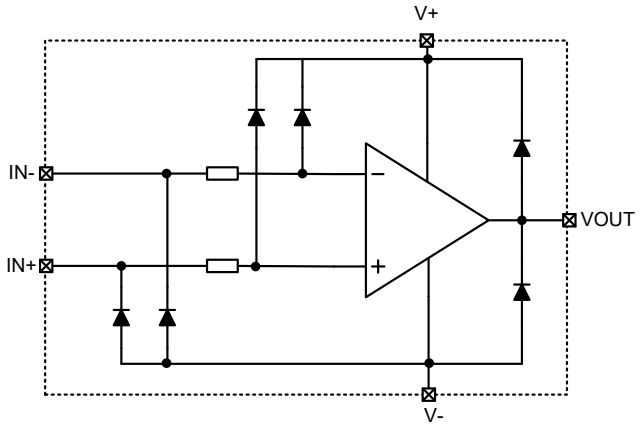



Figure 8-11 Internal ESD Equipment Model

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin.

Electrostatic Discharge (ESD) is defined the transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is regarded as a high voltage(kV), short duration event(1-100ns). Besides, it is fast edges and lower power event.

But unlike ESD problems, EOS is another common device problem. Electrical Over Stress (EOS) is defined the exposure of an item to current or voltage beyond its maximum ratings.

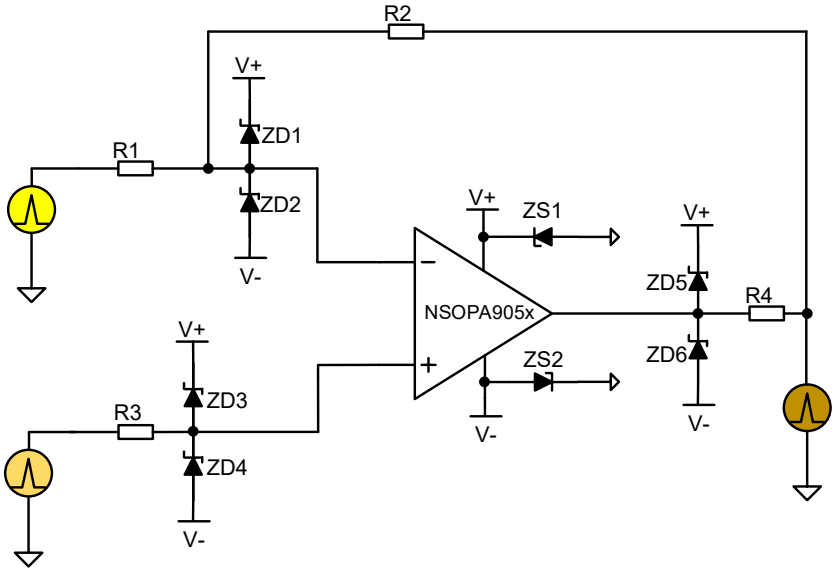



Figure 8-12 External component to enhance EOS performance

Figure 8-12 shows how to use external components to enhance the circuitry robustness.

1. ZDx are small signal Schottky diodes. Using power Schottky for power operational amplifier. Diodes limits EOS Voltage to [(V+) +0.3V] or [(V-)-0.3V].
2. ZS1 and ZS2 are Zener diodes or unipolar semiconductor Transient Voltage Suppressors (TVS). They prevent device supply over-voltage, provide reverse polarity protection, and provide a current path for Iq if one supply floats.
3. R1, R2 limit current through SD1, SD2.
4. R3 limits current through SD3, SD4.
5. R4 limits current through SD5, SD6.R4 is inside the feedback loop adding little error at output voltage.
6. **Check Absolute Maximum Ratings before using devices and never violate the Absolute Maximum Ratings.**

# 9. Application

## 9.1. Active Filter

NSOPA905x can be configured into different types of filters for processing complex signals. Here is a brief explanation of Sallen-key filter type.

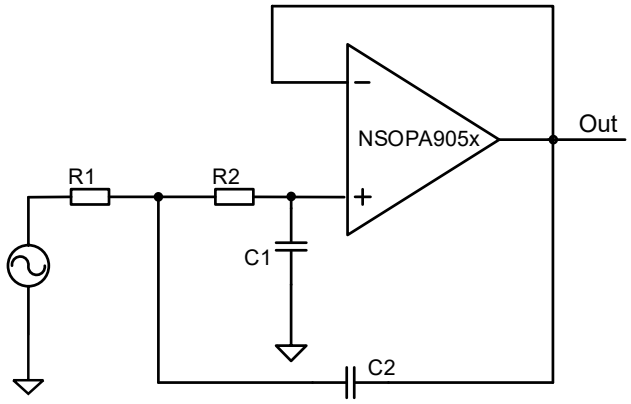



Figure 9-1 2nd order Sallen-key filter

The transfer function of this circuit can be derived as:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (1)$$

The 1kHz low pass filter is taken as a design example. By setting R1=9.1kΩ, R2=13 kΩ, C1=10nF and C2=20.5nF, we can get the amplitude-frequency and phase-frequency curves as follows.

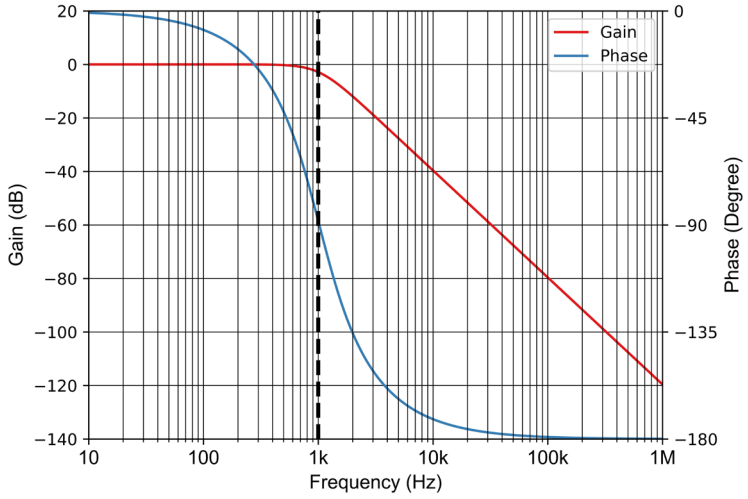



Figure 9-2 amplitude-frequency and phase-frequency curves

## 9.2. High-Side Current Sensing

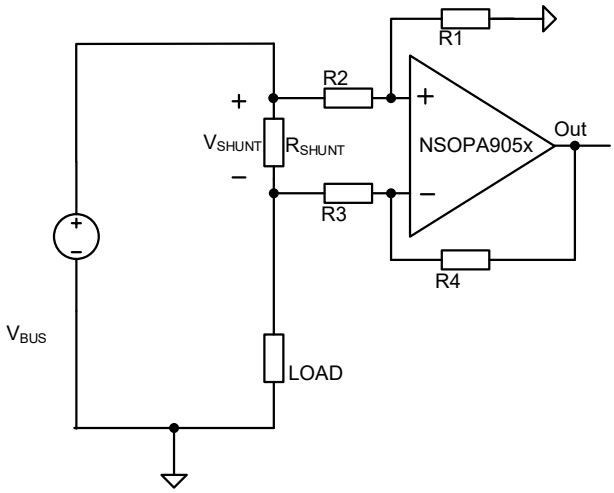



Figure 9-3 High-Side Current Sensing

NSOPA905x can be used in the high-side current sensing application.

When designing high-side current sensing circuits, the common-mode voltage of the op amp must be considered. The common-mode voltage is set by the bus voltage and the resistor divider formed by resistors R1 and R2 (shown in Figure 1) and is calculated using Equation 1 below.

$$\mathrm{Vcm} = \frac{\mathrm{R1}}{\mathrm{R1} + \mathrm{R2}} \times \mathrm{V_{BUS}} \quad (1)$$

Typically, R1=R4, R2=R3. To ensure accuracy, it is important that R1 and R4 and R2 to R3 match closely. Any mismatch may result in gain and CMRR errors. It is recommended to minimize these errors by using matched resistors with an accuracy of 0.1% for external circuitry.

In low-power application, the consumption of resistor shall be taken into consideration.

$$\mathrm{GAIN} = \frac{\mathrm{R4}}{\mathrm{R3}} \quad (2)$$

The input offset voltage must also be considered when determining the accuracy of the solution. Input offset voltage is inherent to the op amp and changes the expected output voltage, as shown in Equation 3.

This error can be significant if the offset voltage is close to the same value as the voltage across the shunt resistor ($V_{SHUNT}$). It is recommended to use op amps with lower inherent offset voltages to minimize system errors.

$$\mathrm{V_{OUT}} = \mathrm{GAIN} \times \mathrm{V_{SHUNT}} + (\mathrm{GAIN} + 1) \times \mathrm{V_{OS}} \quad (3)$$

# 10. Layout Guidance

## 10.1. Guidelines

Poor op amp PCB layout will deteriorate the chip parameters, or even worse, cause it to work abnormally. For better performance, some tips should be considered.

• Noise can propagate into the analog circuitry through the board's power connections and to the power pins of the op amp itself. Bypass capacitors are used to reduce coupled noise by providing a low impedance path to ground.

– Connect a low ESR 0.1µF ceramic bypass capacitor between each supply pin and ground as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single-supply applications.

• To reduce parasitic coupling, keep input traces as far away from power supply or output traces as possible. If these traces cannot be kept separate, route them at a 90-degree angle

It's much better to run overly sensitive traces than to run traces parallel to noisy traces.

• External components should be located as close to the device as possible, as shown in following figure. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.

• Keep input traces as short as possible. Remember, the input traces are the most sensitive parts of the circuit.

• For best performance, cleaning is recommended after PCB board assembly.

## 10.2. Example

A single channel is shown as follow. The rest channels should be handled with identical way but not shown in the figure.

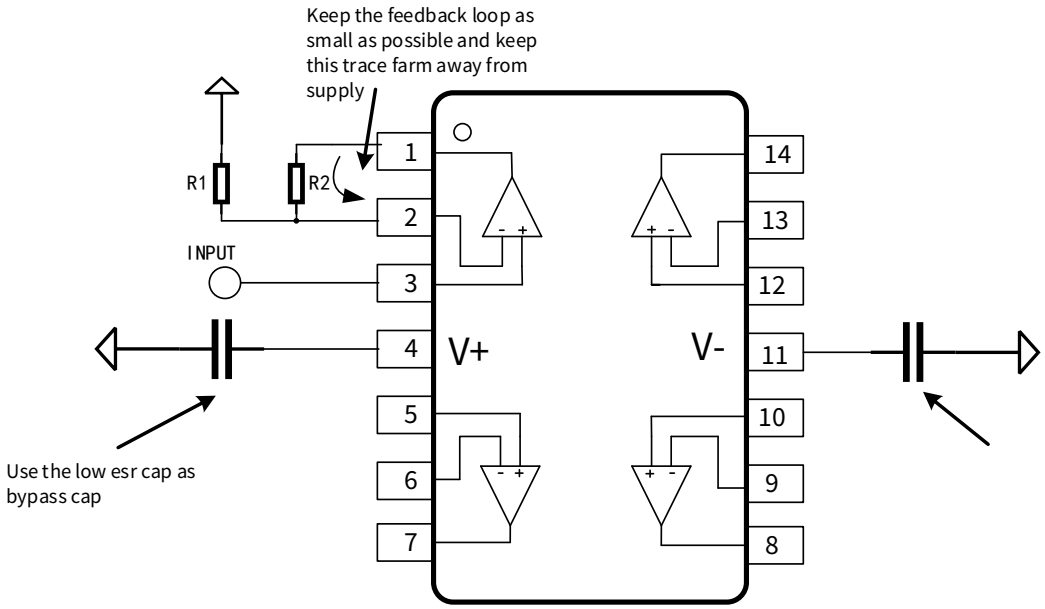
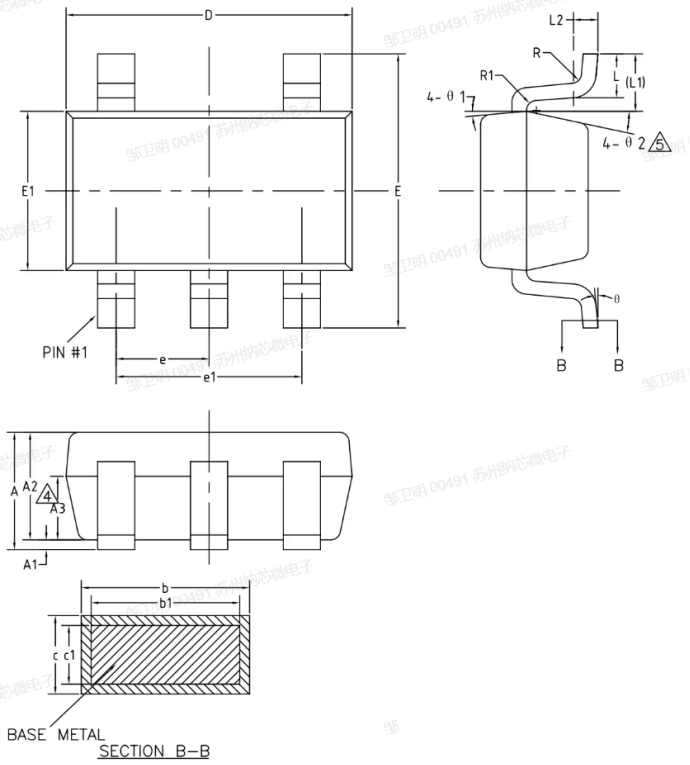



Figure 10-1 Layout example

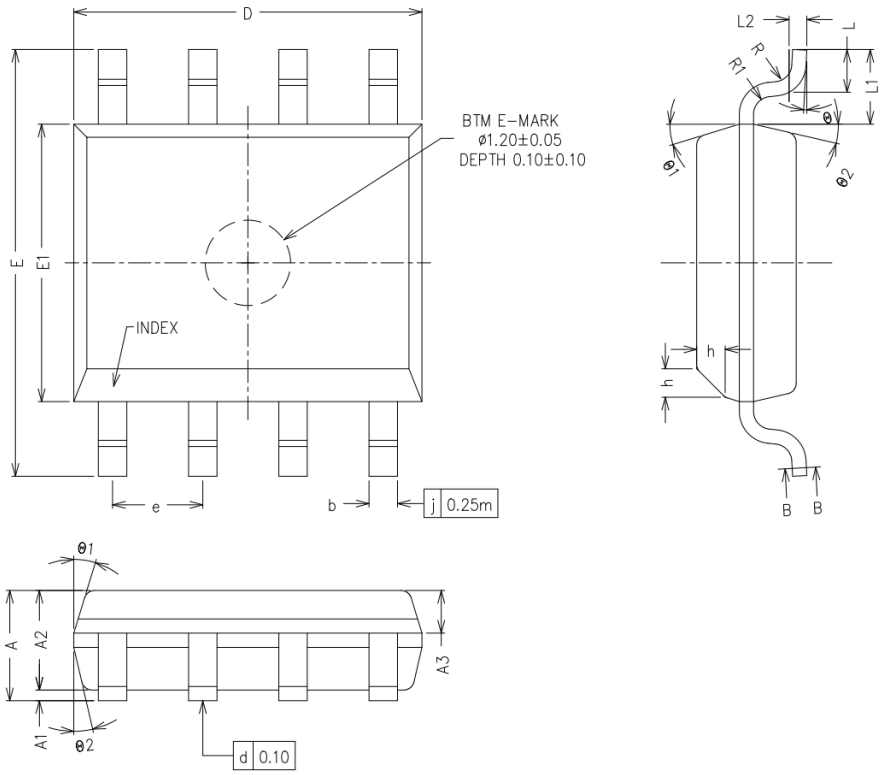
# 11. Package Information

## 11.1. SOT-23(5)



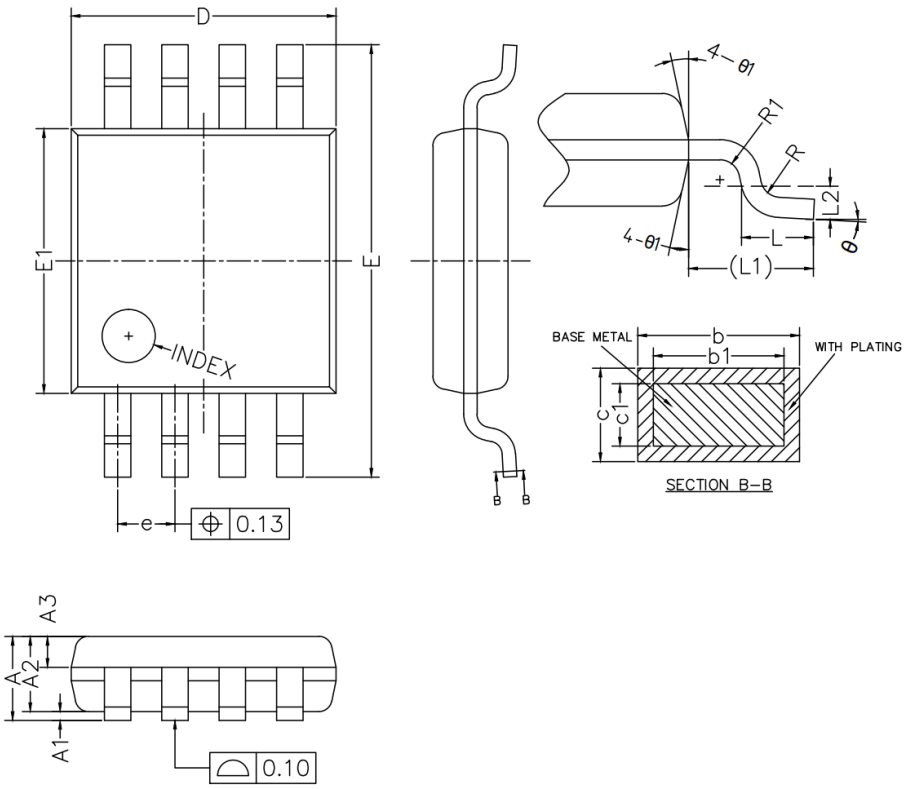

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | — — | 1.25 | — — | 0.049 |
| A1 | — — | 0.15 | — — | 0.006 |
| A2 | 1.00 | 1.20 | 0.039 | 0.047 |
| A3 | 0.60 | 0.70 | 0.024 | 0.028 |
| b | 0.36 | 0.50 | 0.014 | 0.020 |
| b1 | 0.36 | 0.45 | 0.014 | 0.018 |
| c | 0.14 | 0.20 | 0.006 | 0.008 |
| c1 | 0.14 | 0.16 | 0.006 | 0.006 |
| D | 2.826 | 3.026 | 0.111 | 0.119 |
| E | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.526 | 1.726 | 0.060 | 0.068 |
| e | 0.90 | 1.00 | 0.035 | 0.039 |
| e1 | 1.80 | 2.00 | 0.071 | 0.079 |
| L | 0.35 | 0.60 | 0.014 | 0.024 |
| L1 | 0.59REF | | 0.023REF | |
| L2 | 0.25BSC | | 0.010BSC | |
| R | 0.10 | — — | 0.004 | — — |
| R1 | 0.10 | 0.25 | 0.004 | 0.010 |
| θ | 0° | 8° | 0° | 8° |
| θ1 | 3° | 7° | 3° | 7° |
| θ2 | 6° | 14° | 6° | 14° |

### 11.2. SOP (8)



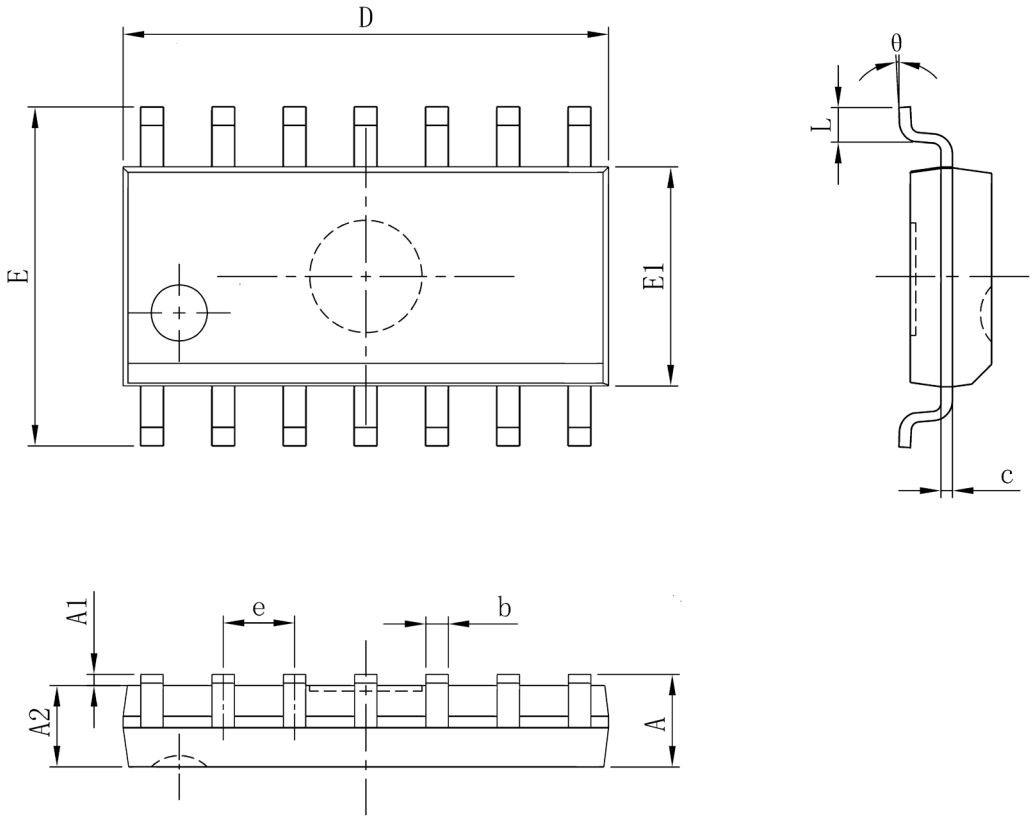

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | — — | 1.75 | — — | 0.069 |
| A1 | 0.05 | 0.25 | 0.002 | 0.01 |
| A2 | 1.30 | 1.50 | 0.051 | 0.059 |
| A3 | 0.50 | 0.70 | 0.020 | 0.028 |
| b | 0.38 | 0.47 | 0.015 | 0.019 |
| b1 | 0.37 | 0.40 | 0.015 | 0.016 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.15 | 0.157 |
| e | 1.17 | 1.37 | 0.046 | 0.054 |
| L | 0.45 | 0.80 | 0.018 | 0.031 |
| L1 | 1.04REF | | 0.041REF | |
| L2 | 0.25BSC | | 0.010BSC | |
| R | 0.07 | — — | 0.003 | — — |
| R1 | 0.07 | — — | 0.003 | — — |
| h | 0.30 | 0.50 | 0.012 | 0.020 |
| θ | 0° | 8° | 0° | 8° |
| θ1 | 15° | 19° | 15° | 19° |
| θ2 | 11° | 15° | 11° | 15° |

### 11.3. MSOP (8)



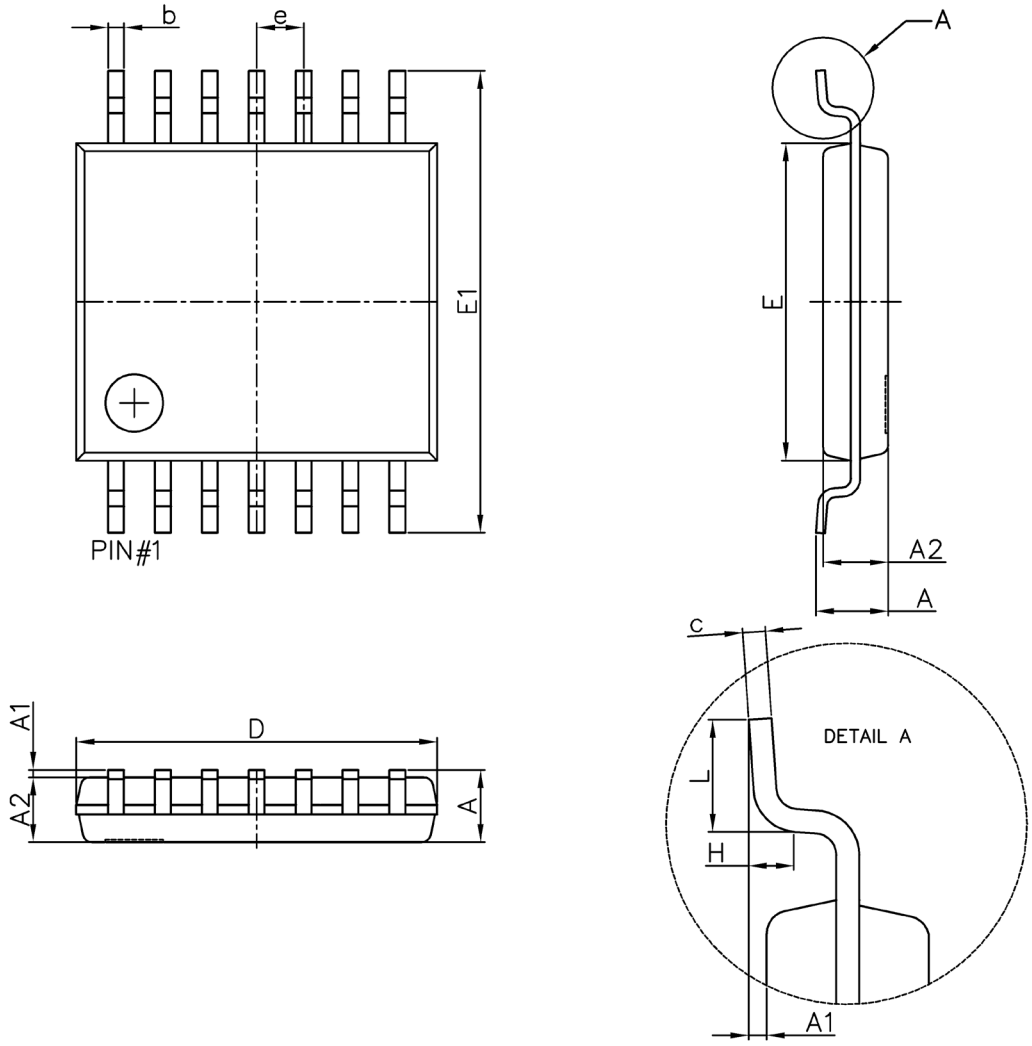

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | — — | 1.10 | — — | 0.043 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.75 | 0.95 | 0.030 | 0.037 |
| A3 | 0.30 | 0.40 | 0.012 | 0.016 |
| b | 0.25 | 0.38 | 0.010 | 0.015 |
| b1 | 0.24 | 0.33 | 0.009 | 0.013 |
| c | 0.15 | 0.20 | 0.006 | 0.008 |
| c1 | 0.14 | 0.16 | 0.006 | 0.0062 |
| D | 2.90 | 3.10 | 0.114 | 0.122 |
| E | 4.75 | 5.05 | 0.187 | 0.199 |
| E1 | 2.90 | 3.10 | 0.114 | 0.122 |
| e | 0.55 | 0.75 | 0.022 | 0.030 |
| L | 0.40 | 0.70 | 0.016 | 0.028 |
| L1 | 0.95REF | | 0.037(BSC) | |
| L2 | 0.25BSC | | 0.010 | |
| R | 0.07 | — — | 0° | 8° |
| R1 | 0.07 | — — | 0.003 | — — |
| θ | 0° | 8° | 0° | 8° |
| θ1 | 9° | 15° | 9° | 15° |

### 11.4. SOP (14)



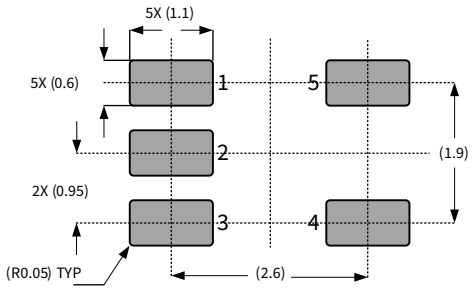

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | — — | 1.75 | — — | 0.069 |
| A1 | 0.1 | 0.25 | 0.004 | 0.01 |
| A2 | 1.25 | — — | 0.049 | — — |
| b | 0.31 | 0.51 | 0.012 | 0.02 |
| c | 0.1 | 0.25 | 0.004 | 0.01 |
| D | 8.45 | 8.85 | 0.333 | 0.348 |
| E | 5.8 | 6.2 | 0.228 | 0.244 |
| E1 | 3.8 | 4 | 0.15 | 0.157 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| L | 0.4 | 0.016 | 0.016 | 0.05 |
| θ | 0° | 0° | 0° | 8° |

### 11.5. TSSOP (14)

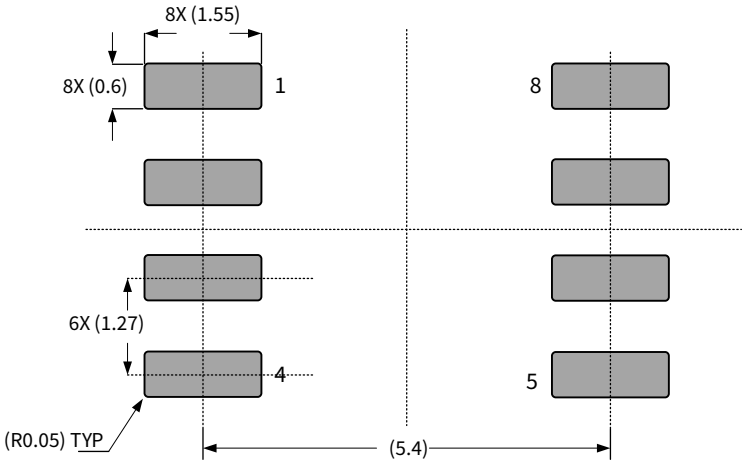



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| D | 4.9 | 5.1 | 0.193 | 0.201 |
| E | 4.3 | 4.5 | 0.169 | 0.177 |
| b | 0.19 | 0.3 | 0.007 | 0.012 |
| c | 0.09 | 0.2 | 0.004 | 0.008 |
| E1 | 6.25 | 6.55 | 0.246 | 0.258 |
| A | — | 1.2 | — | 0.047 |
| A2 | 0.8 | 1 | 0.031 | 0.039 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| e | 0.65 (BSC) | | 0.026 (BSC) | |
| L | 0.5 | 0.7 | 0.02 | 0.028 |
| H | 0.25(TYP) | | 0.01(TYP) | |
| θ | 1° | 7° | 1° | 7° |

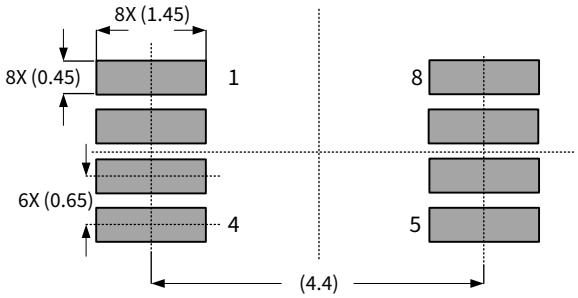
## 11.6. Example of Solder Pads Dimensions



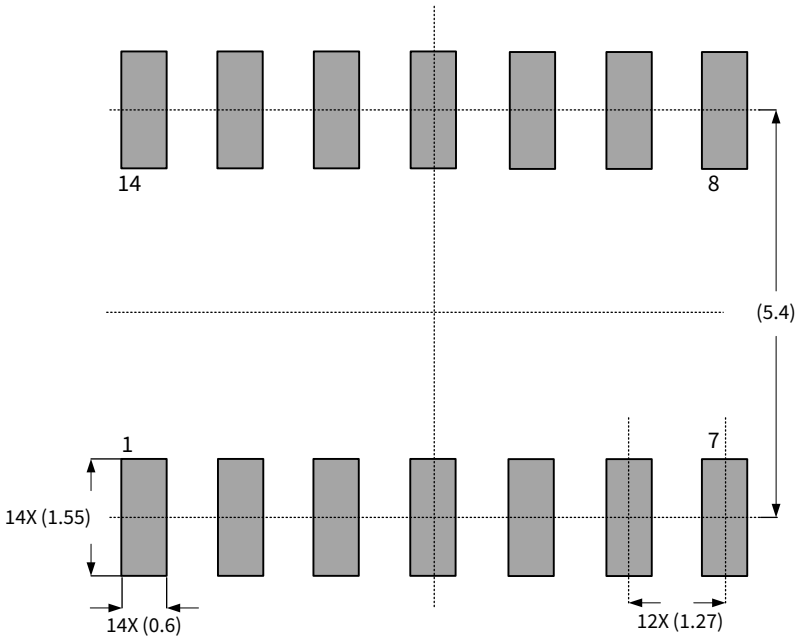

SOT23-5L



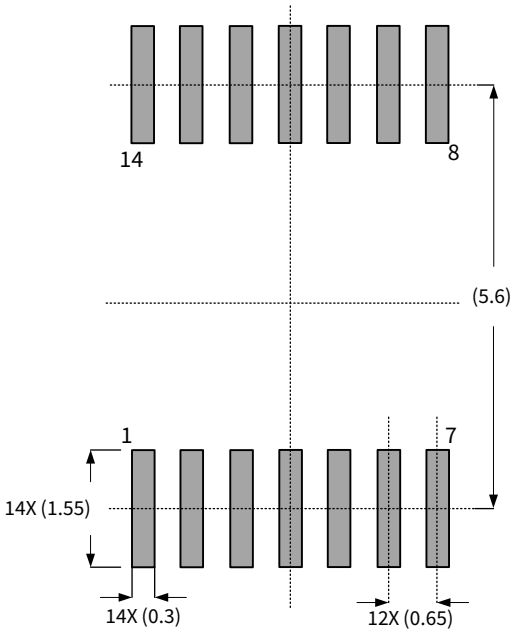

SOP8




MSOP8




SOP14




TSSOP14

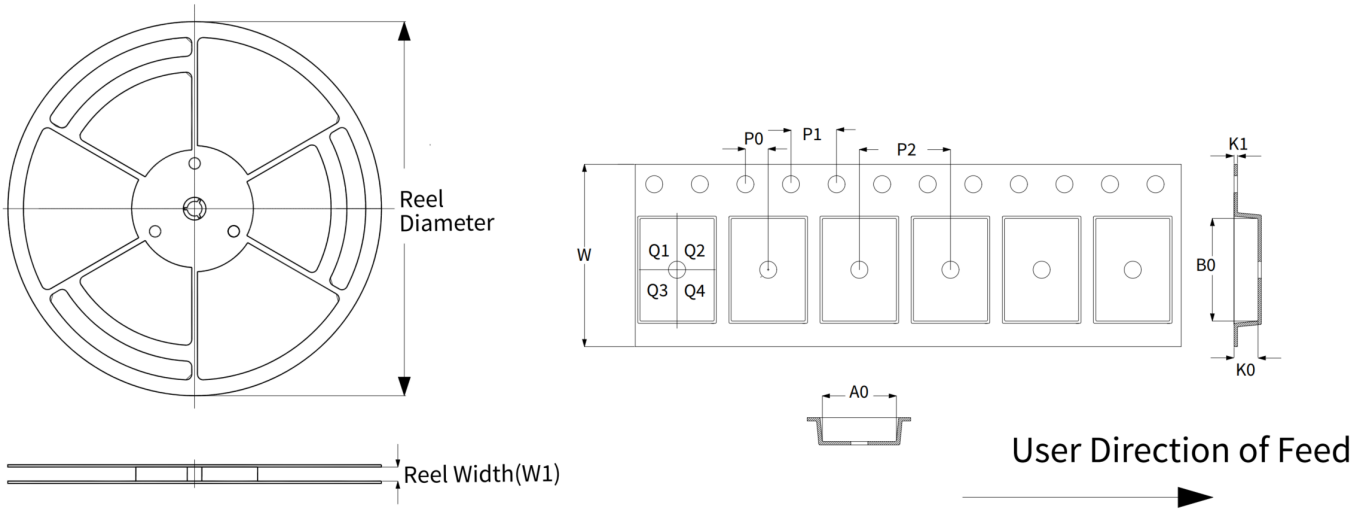
Note:

1. Unit: mm.

# 12. Ordering Information

| *Part Number* | *Package* | *MSL Level* | *Op Temp (°C)* | *SPQ* |
|---|---|---|---|---|
| NSOPA9051-DSTAR | SOT-23 (5) | 3 | -40~+125 | 3000 |
| NSOPA9051-DSPR | SOP (8) | 3 | -40~+125 | 2500 |
| NSOPA9052-DSPR | SOP (8) | 3 | -40~+125 | 2500 |
| NSOPA9052-DMSR | MSOP (8) | 3 | -40~+125 | 2500 |
| NSOPA9054-DSPKR | SOP (14) | 3 | -40~+125 | 2500 |
| NSOPA9054-DTSKR | TSSOP (14) | 3 | -40~+125 | 4000 |
| Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature. | | | | |

## 13. Tape and Reel Information




| Device | Reel Diameter | Reel Width(W1) | W | A0 | B0 | P0 | P1 | P2 | K0 | K1 | PIN1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| NSOPA9051-DSTAR | 178 | 8.4 | 8.0 | 3.3 | 3.2 | 2.0 | 4.0 | 4.0 | 1.4 | 0.23 | Q3 |
| NSOPA9051-DSPR | 330 | 12.4 | 12.0 | 6.6 | 5.5 | 2.0 | 4.0 | 8.0 | 2.1 | 0.3 | Q1 |
| NSOPA9052-DSPR | 330 | 12.4 | 12.0 | 6.6 | 5.5 | 2.0 | 4.0 | 8.0 | 2.1 | 0.3 | Q1 |
| NSOPA9052-DMSR | 330 | 12.4 | 12.0 | 5.25 | 3.35 | 2.0 | 4.0 | 8.0 | 1.25 | 0.3 | Q1 |
| NSOPA9054-DSPKR | 330 | 16.4 | 16.0 | 6.60 | 9.3 | 2.0 | 4.0 | 8.0 | 2.1 | 0.3 | Q1 |
| NSOPA9054-DTSKR | 330 | 16.4 | 12.0 | 6.85 | 5.4 | 2.0 | 4.0 | 8.0 | 1.6 | 0.3 | Q1 |

Note:

2. All dimensions are nominal.
3. The picture is only for reference. Please make the object as the standard.
4. Unit: mm.

# 14. Revision History

| Revision | Description | Date |
|---|---|---|
| V1.0 | Initial version | 2024/05 |
| V1.1 | Add example of solder pads dimensions<br>Add reflow note in order information table | 2024/08 |

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