NOVOSENSE
纳芯微电子

NCA9548

8-channel I2C-bus switch with reset

Datasheet (EN) 1.1

Product Overview

The NCA9548 is an octal bidirectional translating switch controlled via the I^2C bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset (RESET) input allows the NCA9548 to recover from a situation in which one of the downstream I^2C buses is stuck in a low state. Pulling RESET low resets the I^2C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the NCA9548. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Key Features

- 1-of-8 Bidirectional Translating Switches
- I^2C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Address Terminals, Allowing up to Eight Devices on the I^2C Bus
- Channel Selection via I^2C Bus, in Any Combination
- Power-Up with All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - – 2000-V Human-Body Model (A114-A)
  - – 1000-V Charged-Device Model (C101)

Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I^2C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Device Information

Part Number	*Package*	*Body Size*
NCA9548-DTSXR	TSSOP24	7.8mm*4.4mm

Functional Block Diagrams

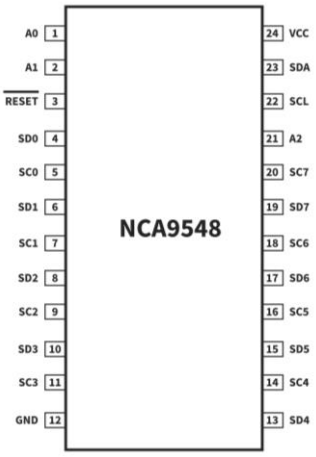

Figure 1. NCA9548 Block Diagram

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1. Pin Configuration and Functions

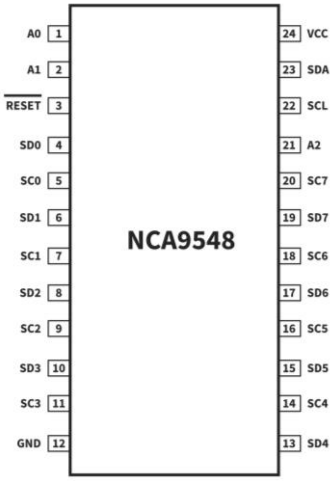


Figure 1.1 NCA9548 Package

Table 1.1 Pin Configuration and Description

Symbol	*Pin*	*Description*
A0	1	Address input 0. Connect directly to VCC or ground.
A1	2	Address input 1. Connect directly to VCC or ground.
RESET	3	Active-low reset input. Connect to VCC or V_{DPUM}[1] through a pull-up resistor if not used.
SD0	4	Serial data 0. Connect to V_{DPU0}[1] through a pull-up resistor.
SC0	5	Serial clock 0. Connect to V_{DPU0}[1] through a pull-up resistor.
SD1	6	Serial data 1. Connect to V_{DPU1}[1] through a pull-up resistor.
SC1	7	Serial clock 1. Connect to V_{DPU1}[1] through a pull-up resistor.
SD2	8	Serial data 2. Connect to V_{DPU2}[1] through a pull-up resistor.
SC2	9	Serial clock 2. Connect to V_{DPU2}[1] through a pull-up resistor.
SD3	10	Serial data 3. Connect to V_{DPU3}[1] through a pull-up resistor.
SC3	11	Serial clock 3. Connect to V_{DPU3}[1] through a pull-up resistor.
GND	12	Ground
SD4	13	Serial data 4. Connect to V_{DPU4}[1] through a pull-up resistor.
SC4	14	Serial clock 4. Connect to V_{DPU4}[1] through a pull-up resistor.
SD5	15	Serial data 5. Connect to V_{DPU5}[1] through a pull-up resistor.
SC5	16	Serial clock 5. Connect to V_{DPU5}[1] through a pull-up resistor.
SD6	17	Serial data 6. Connect to V_{DPU6}[1] through a pull-up resistor.
SC6	18	Serial clock 6. Connect to V_{DPU6}[1] through a pull-up resistor.
SD7	19	Serial data 7. Connect to V_{DPU7}[1] through a pull-up resistor.

Symbol	Pin	Description
SC7	20	Serial clock 7. Connect to V_{DPU7}[1] through a pull-up resistor.
A2	21	Address input 2. Connect directly to VCC or ground.
SCL	22	Serial clock line. Connect to V_{DPUM}[1] through a pull-up resistor.
SDA	23	Serial data line. Connect to V_{DPUM}[1] through a pull-up resistor.
VCC	24	Supply power

[1] V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C master reference voltage and V_{DPU0}–V_{DPU3} are the slave channel reference voltages.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Conditions
Supply Voltage	V_{CC}	-0.5	7	V	
Input/output Voltage	V_I/V_O	-0.5	7	V	
Input current	I_I		±25	mA	
Output current	I_O		±25	mA	V_O<0V
Continuous current through VCC or GND	I_{CC}		±100	mA	
Operating Temperature	Topr	-40	105	℃	
Storage Temperature	Tstg	-65	150	℃	
Electrostatic discharge	HBM		±2000	V	
	CDM		±1000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	1.65	5.5	V	
High-level input voltage	V_{IH}	0.7*V_{CC}	6	V	SCL, SDA
		0.7*V_{CC}	V_{CC}+0.5	V	A2, A1, A0, INT3–INT0, RESET
Low-level input voltage	V_{IL}	-0.5	0.3*V_{CC}	V	SCL, SDA
		-0.5	0.3*V_{CC}	V	A2, A1, A0, INT3–INT0, RESET
Operating free-air temperature	T_A	-40	105	℃	

4. Thermal Information

Parameters	*Symbol*		*Unit*
Junction-to-ambient thermal resistance	θ_{JA}	115.3	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	48.7	℃/W
Junction-to-board thermal resistance	θ_{JB}	66.4	℃/W

5. Specifications

5.1. Electrical Characteristics

V_{CC} = 1.65V to 5.5V; T_{amb} = -40℃ to +105℃; unless otherwise noted. Typical specification are at T_A=25℃,V_{CC}=3.3V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Supply						
Supply voltage Range	V_{CC}	1.65	-	5.5	V	
Power on Reset rising	V_{PORR}	-	1.15	1.4	V	no load; V_I = V_{CC} or GND
Power on Reset falling	V_{PORF}	0.9	1.08		V	no load; VI = V_{CC} or GND
Supply current	I_{CC}	-	-	10	μA	Operating mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load; f_{SCL} = 100 kHz
Standby current	I_{stb}	-	0.7	5	μA	Standby mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load
Input SCL; Input/Output SDA						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	When V_{CC}=1.65V-2.3V, the minimum value of VIH is 0.8*V_{CC}
LOW-level output current	I_{OL}	2.5	15	-	mA	V_{OL} = 0.4 V
		5	20		mA	V_{OL}=0.6V
Input leakage current	I_L	-1	-	+1	μA	V_I = V_{CC} or GND
Input capacitance	C_i	-	15		pF	V_I = GND
Select inputs A0,A1,A2,RESET						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	When V_{CC}=1.65V-2.3V, the minimum value of VIH is 0.8*V_{CC}

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Leakage current	I_L	-1	-	1	μA	V_I = V_{CC} or GND
Input capacitance	C_i	-	1.6	3	pF	V_I = GND
Pass gate						
On-state resistance	R_{on}	4	14	20	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 4.5V
		5	16	25	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 3V
		6	19	30	Ω	Vo=0.4 V, I_O = 10 mA, V_{CC} = 2.3V
		10	28	40	Ω	Vo=0.4 V, I_O = 10 mA, V_{CC} = 1.65V
Switch output voltage	$V_{O(SW)}$		3.64		V	V_{CC} = 5 V, $I_{O(SW)}$ = -100uA
		2.6		4.5	V	V_{CC} = 4.5V to 5.5 V, $I_{O(SW)}$ = -100uA
			2.15		V	V_{CC} = 3.3 V, $I_{O(SW)}$ = -100uA
		1.6		2.8	V	V_{CC} = 3 V to 3.6 V, $I_{O(SW)}$ = -100uA
			1.46		V	V_{CC} = 2.5 V, $I_{O(SW)}$ = -100uA
		1		1.9	V	V_{CC} = 2.3 V to 2.7 V, $I_{O(SW)}$ = -100uA
			0.99		V	V_{CC} = 1.8 V, $I_{O(SW)}$ = -100uA
		0.5		1.2	V	V_{CC} = 1.65 V to 1.95 V, $I_{O(SW)}$ = -100uA
Leakage current	I_L	-1	-	+1	μA	V_I = V_{CC} or GND
C_{io}	Input/output capacitance	-	-	6	pF	V_I=GND

5.2. Dynamic Characteristics

Parameters	*Symbol*	*Standard-mode I2C-bus*		*Fast-mode I2C-bus*		*Unit*
		Min	*Max*	*Min*	*Max*	
propagation delay	t_{PD}[1]		0.3		0.3	ns
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
hold time (repeated) START condition	$t_{HD;STA}$[2]	4.0	-	0.6	-	µs
set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
data valid acknowledge time	$t_{VD;ACK}$	0.3	3.45	0.1	0.9	µs
data hold time	$t_{HD;DAT}$[3]	0	-	0	-	ns
data valid time	$t_{VD;DAT}$[4]	300	-	50	-	ns
data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
fall time of both SDA and SCL signals	t_f	-	300	20 + 0.1C_b[5]	300	ns
rise time of both SDA and SCL signals	t_r	-	1000	20 + 0.1C_b[5]	300	ns
pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	50	-	50	ns
$\overline{\text{RESET}}$						
Low-level reset time	$T_{w(rst)L}$	4		4		ns
Reset time[6]	t_{rst}	600		600		ns
Recovery time to START condition		0		0		ns

[1]Pass gate propagation delay is calculated from the 20Ω typical Ron and the 15 pF load capacitance.

[2]After this period, the first clock pulse is generated.

[3]A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4]Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

[5]C_b = total capacitance of one bus line in pF.

[6]The minimum Reset time of the ACK bit is 600ns.

5.3. Parameter Measurement Information

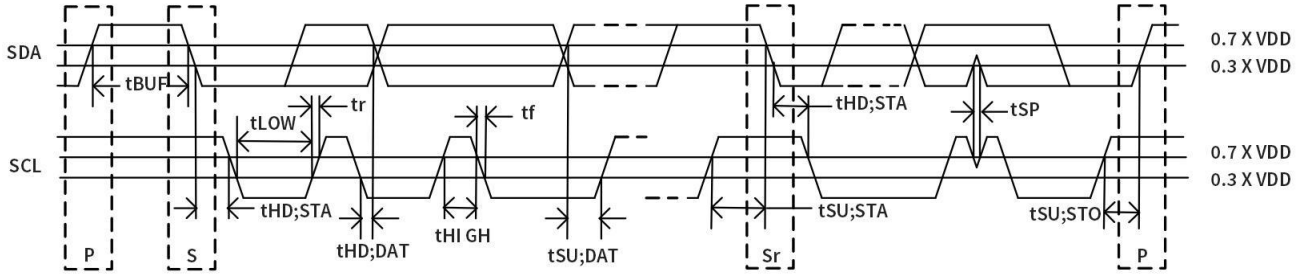


Figure 5.1 Definition of timing on I²C-bus

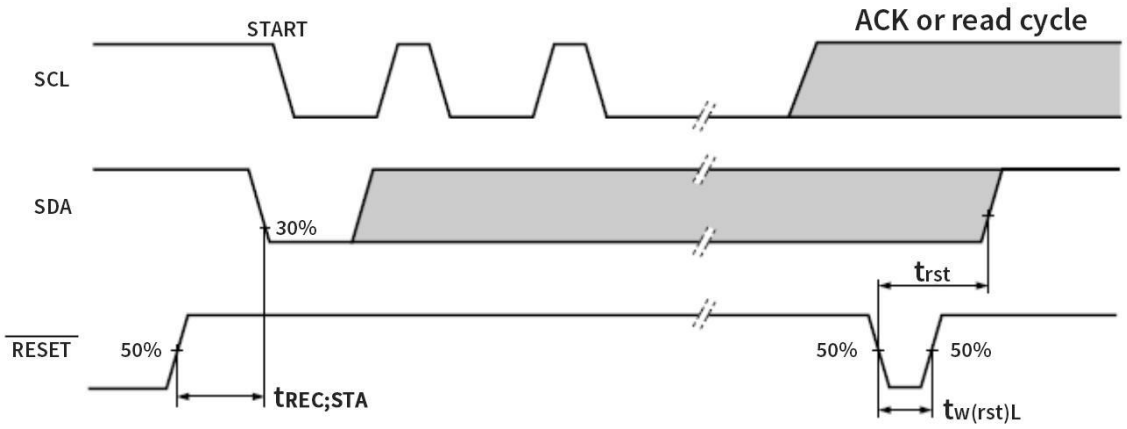


Figure 5.2 Definition of RESET timing

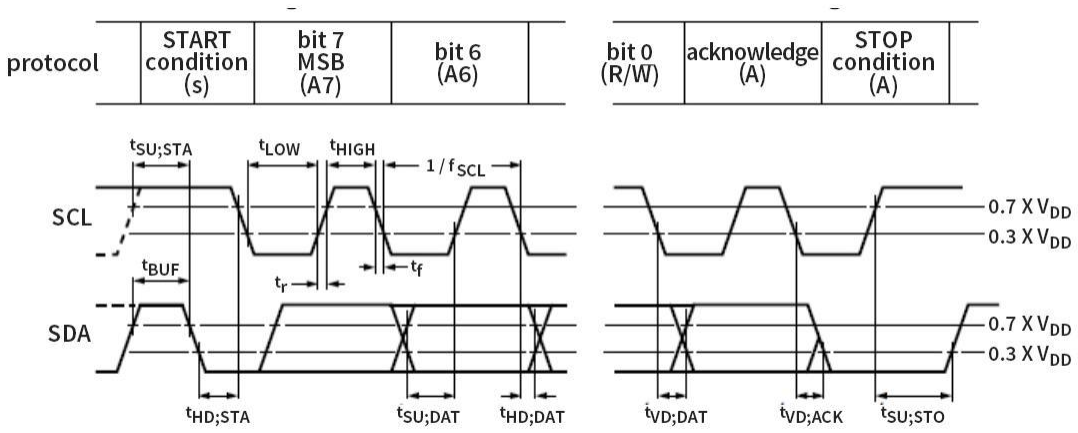
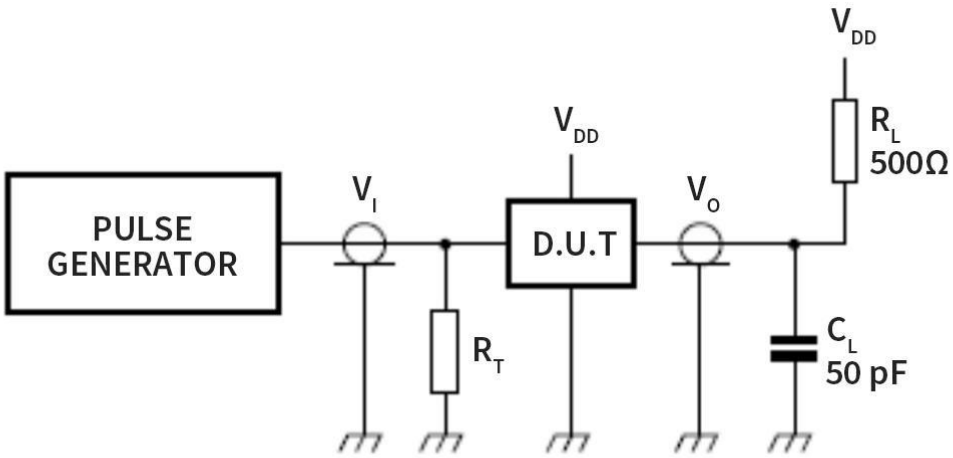


Figure 5.3 I²C-bus timing diagram



Definitions test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Zo of the pulse generator.

Figure 5.4 Test circuitry for switching times

6. Detailed Description

6.1. Overview

The NCA9548 is a 8-channel, bidirectional translating I^2C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC7/SD7. Any individual downstream channel can be selected as well as any combination of the four channels.

The device offers an active-low RESET input which resets the state machine and allows the NCA9548 to recover should one of the downstream I^2C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR) Both the RESET function and a POR will cause all channels to be deselected.

The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 ,A1 and A2 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The NCA9548 may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

6.2. Functional Block Diagram

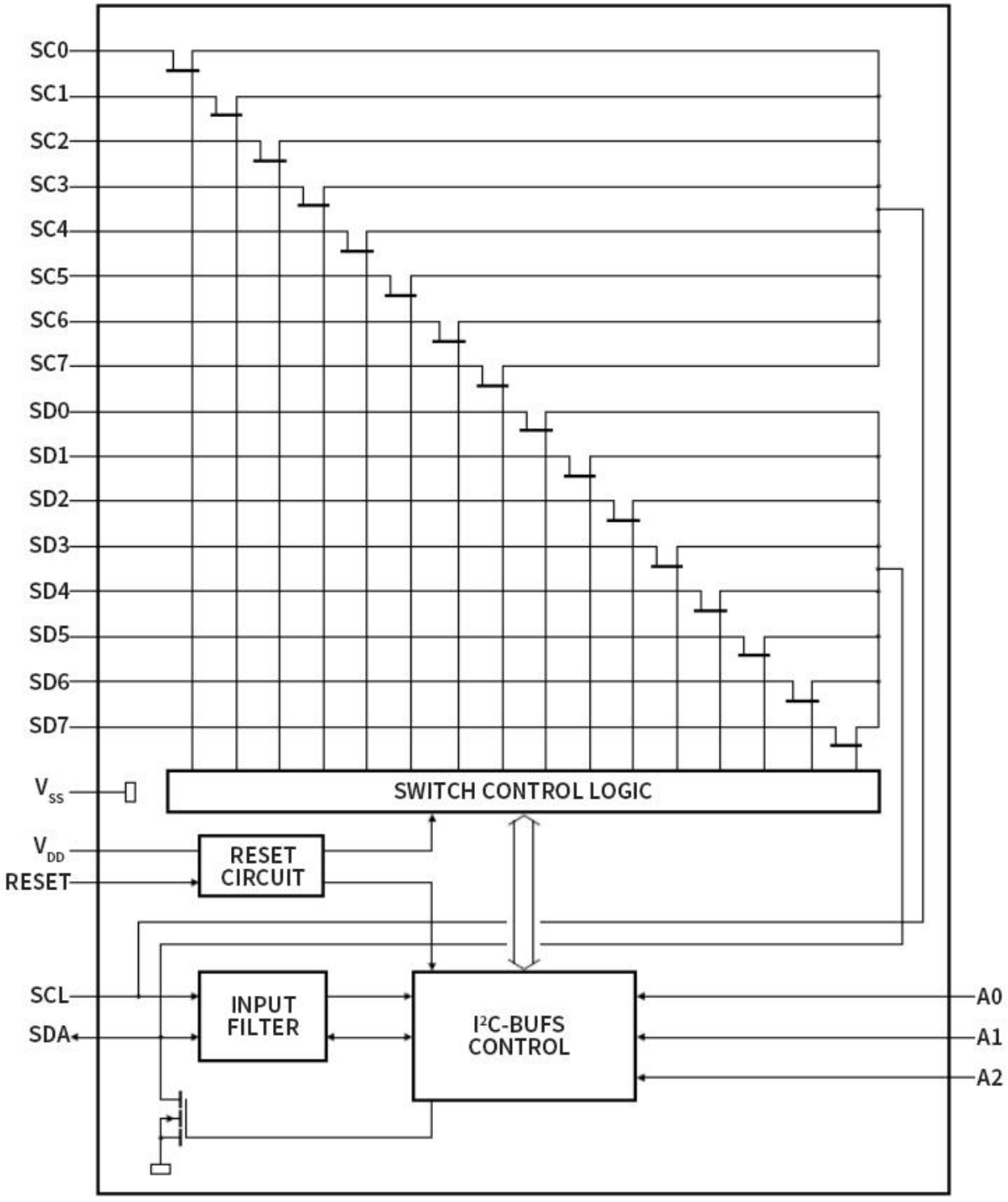


Figure 6.1 NCA9548 Functional block

6.3. Feature Description

The NCA9548 is a 8-channel, bidirectional translating switch for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The NCA9548 features I^2C control using a single 8-bit control register in which each bit controls the enabling and disabling of the 8 switch channels of I^2C data flow.

Depending on the application, voltage translation of the I^2C bus can also be achieved using the NCA9548 to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the NCA9548 can be reset to resume normal operation using the RESET pin feature or by a power-on reset which results from cycling power to the device.

6.4. Device Functional Modes

6.5. RESET Input

The RESET input can be used to recover the NCA9548 from a bus-fault condition. The registers and the I^2C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}.

All channels also are deselected in this case. RESET must be connected to V_{CC} through a pull-up resistor.

6.6. Power-On Reset

When power is applied to VCC, an internal power-on reset holds the NCA9548 in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the NCA9548 registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

6.7. Programming

6.8. I^2C Interface

The I^2C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 6.2)

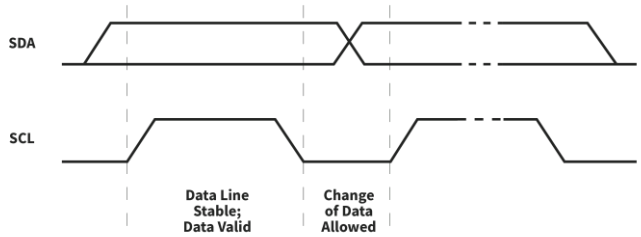


Figure 6.2 Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 6.3).

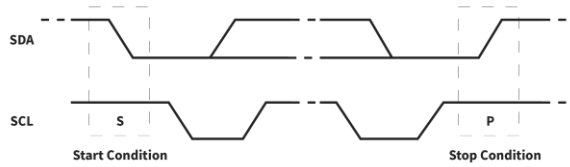


Figure 6.3 Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6.4).

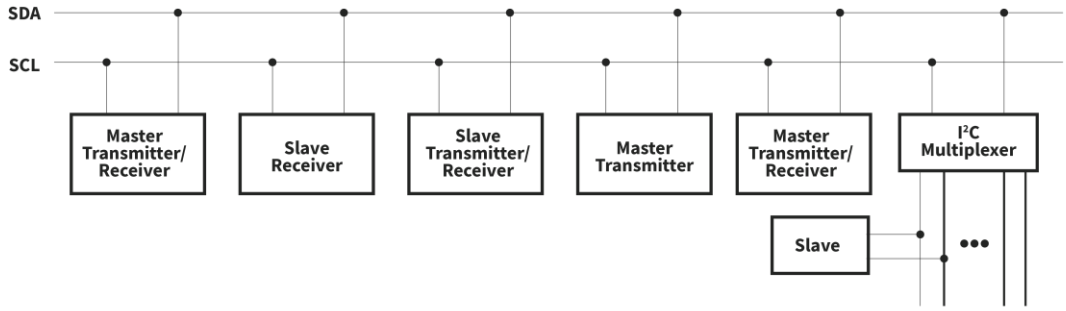


Figure 6.4 System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 6.5). Setup and hold times must be taken into account.

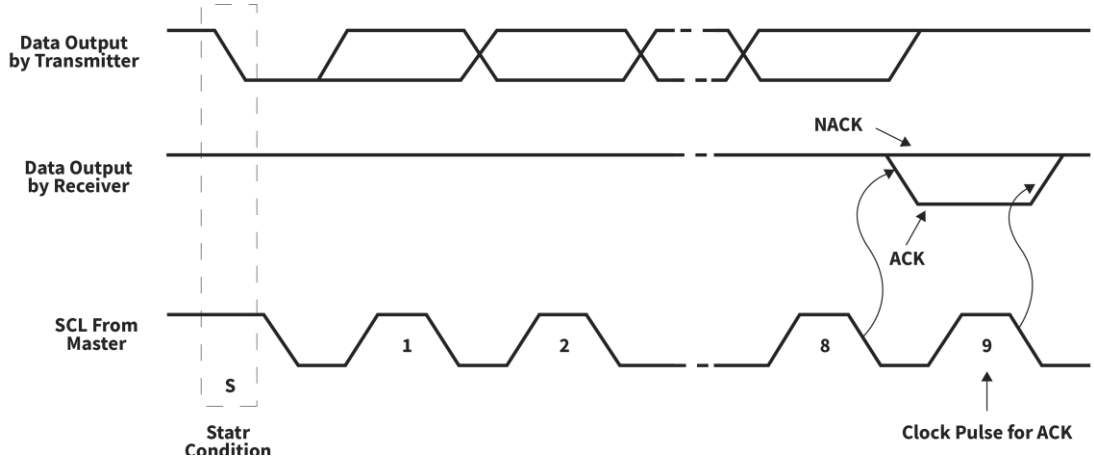


Figure 6.5 Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition. Data is transmitted to the NCA9548 control register using the write mode shown in Figure 6.6.

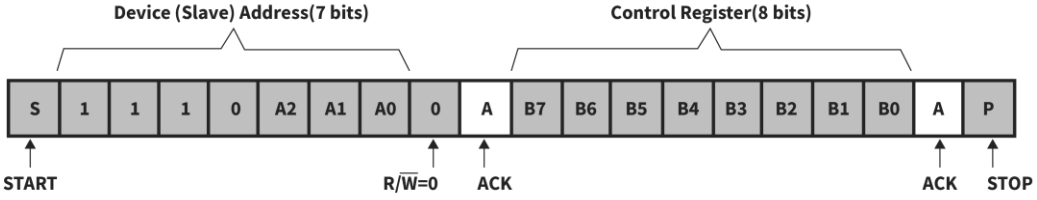


Figure 6.6 Write Control Register

Data is read from the NCA9548 control register using the read mode shown in Figure 6.7.

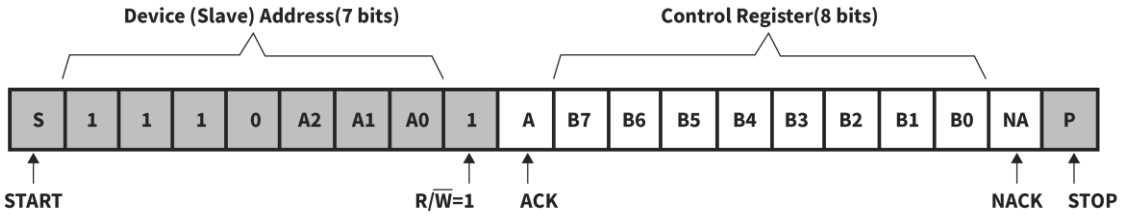


Figure 6.7 Read Control Register

6.9. Control Register

6.10. Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the NCA9548 is shown in Figure 6.8 To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

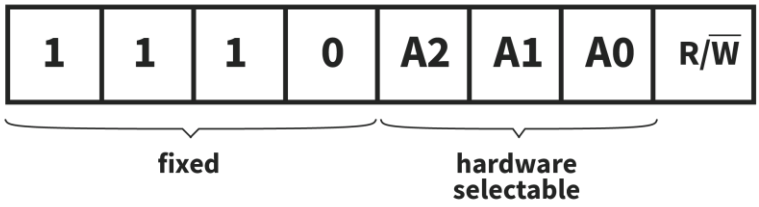


Figure 6.8 NCA9548 Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

6.11. Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the NCA9548, which is stored in the control register (see Figure 6.9). If multiple bytes are received by the NCA9548, it saves the last byte received. This register can be written and read via the I^2C bus.

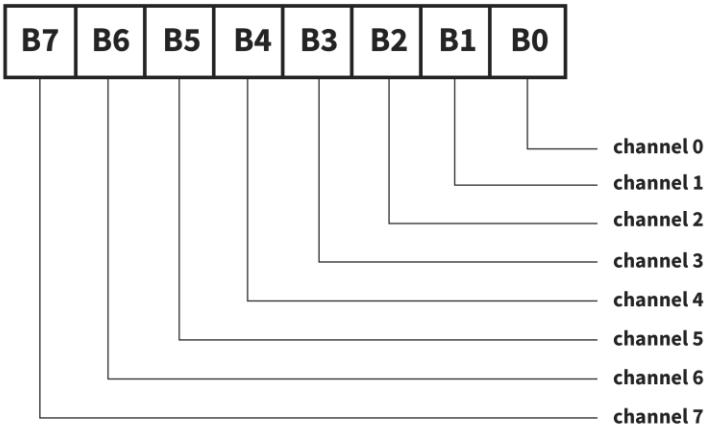


Figure 6.9 Control Register

6.12. Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 6.1). After the NCA9548 has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 6.1. Control Register Write (Channel Selection), Control Register Read (Channel Status)

CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 dinsabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected. power-up/ reset default state

[1] Several channels can be enabled at the same time. For example, B3 = 0, B0 = 0 , others Bx = 1, means that channels 0 and 3 are disabled, and the other channels are enabled. Care should be taken not to exceed the maximum bus capacity.

7. Application and Implementation

Applications of the NCA9548 will contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, to 7. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See Design Requirements and Detailed Design Procedure).

7.1. Typical Application

A typical application of the NCA9548 will contain anywhere from 1 to 9 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU7}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum Vpass is known, Vcc can be selected easily using Figure 7.2 In an application where voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

Figure 7.1 shows an application in which the NCA9548 can be used.

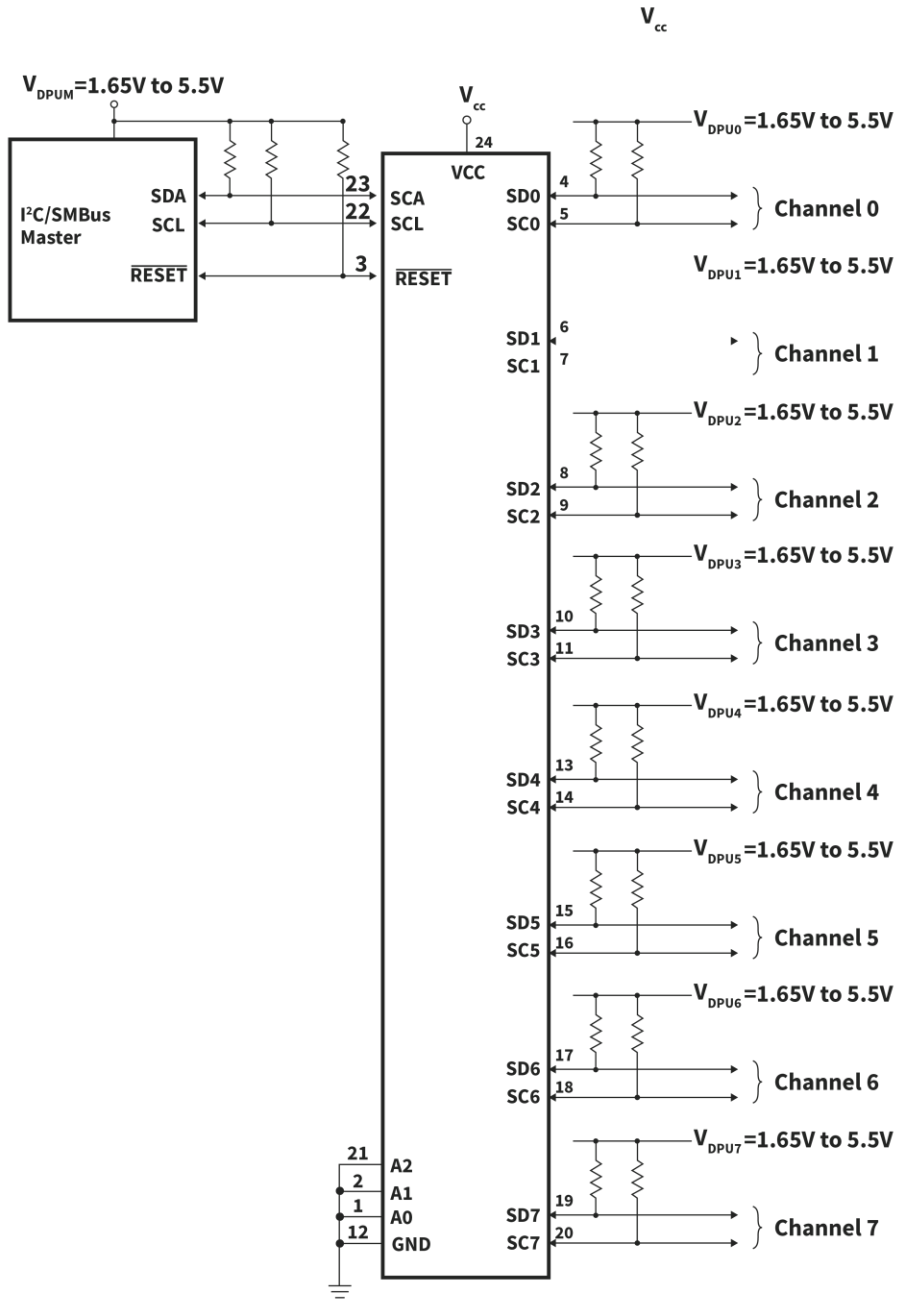


Figure 7.1 Typical Application Schematic

7.2. Design Requirements

The A0 ,A1 and A2 terminals are hardware selectable to control the slave address of the NCA9548. These terminals may be tied directly to GND or VCC in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the NCA9548 are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 7.2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics section of this data sheet). In order for the NCA9548 to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 7.2, Vpass(max) is 2.7 V when the NCA9548A supply voltage is 4 V or lower, so the NCA9548A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 7.1).

7.3. Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUV} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, tr (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the NCA9548, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

7.4. NCA9548 Application Curves

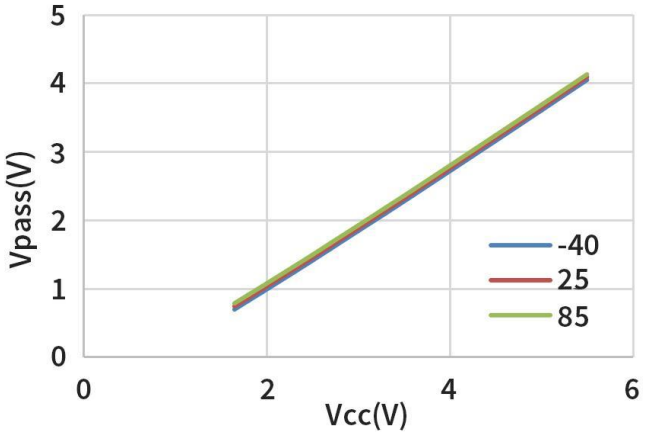
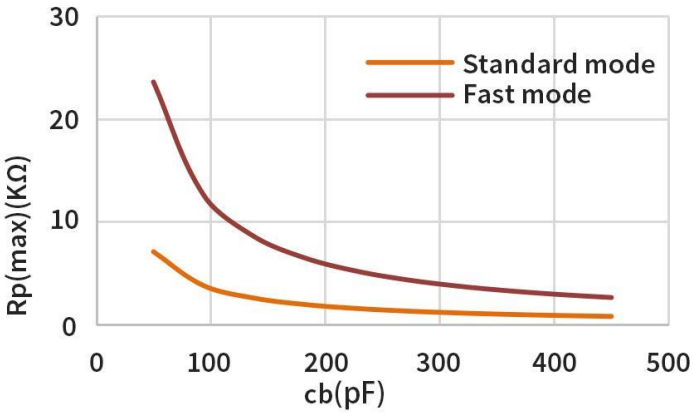
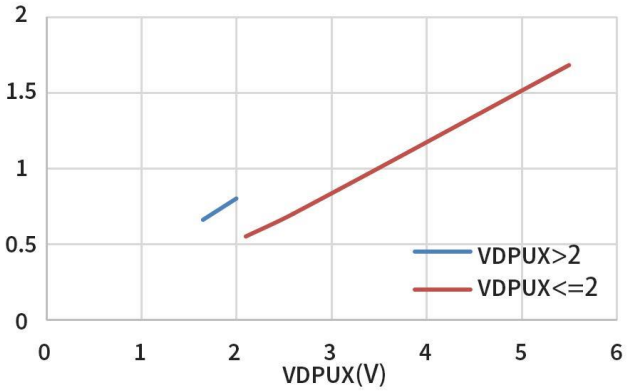


Figure 7.2 Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard mode (fscl=100kHz, tr=1us); Fast mode: (fscl=400kHz,tr=300ns)

Figure 7.3 Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



VOL=0.2*VDPUX, IOL=2mA when VDPUX<=2V; VOL=0.4V, IOL=3mA when VDPUX>2V

Figure 7.4 Minimum Pull-Up resistance ($R_{p(min)}$) vs Pull-up reference voltage (V_{DPUX})

8. Layout

8.1. Layout Guidelines

For PCB layout of the NCA9548, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all VDPUX voltages and VCC could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and INTn) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

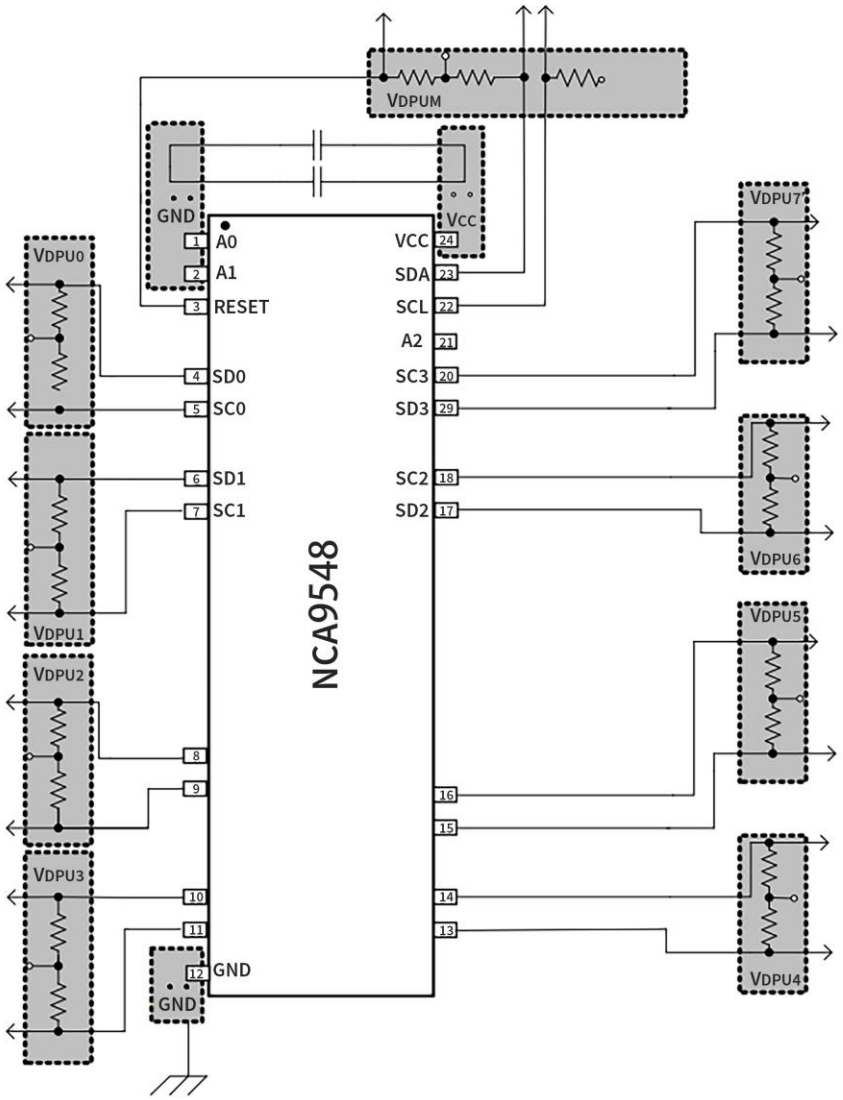
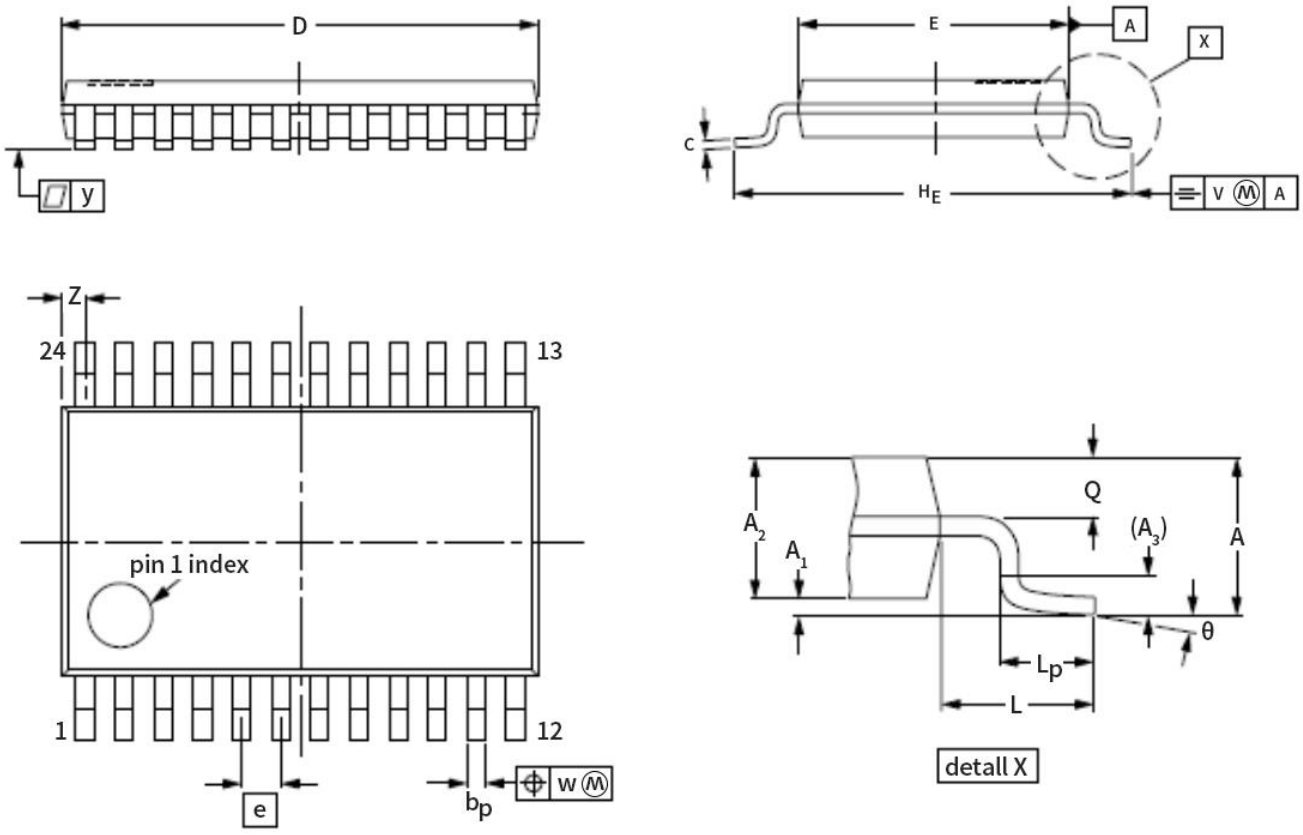


Figure 8.1 Typical Application PCB

9. Package Information



DMENSIONS(mm are the original dimensions)

UNIT	A MAX.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_P	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^0 0^0

Figure 9.1 TSSOP24 Package Shape and Dimension in millimeters

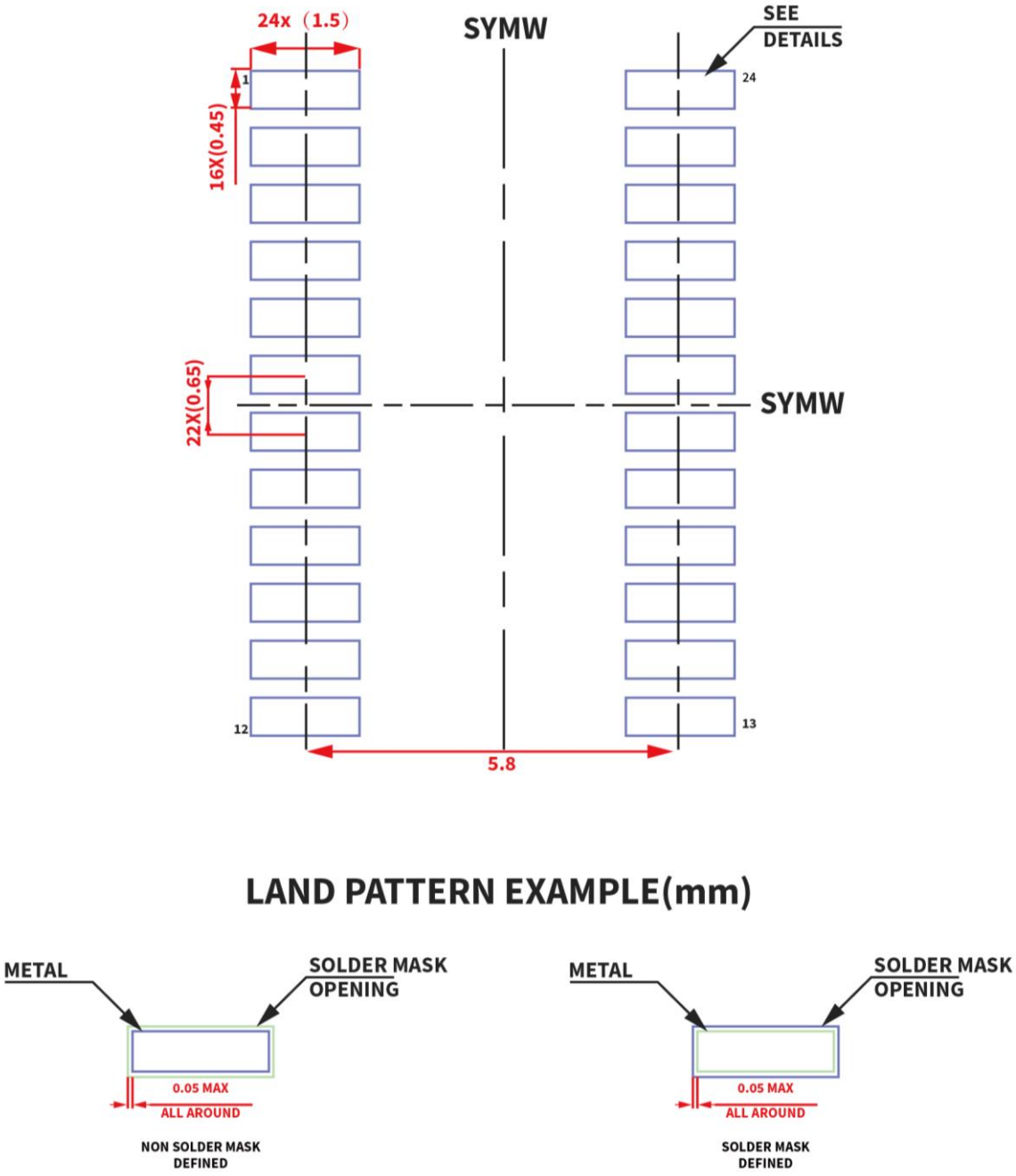


Figure 9.2 TSSOP24 Package Board Layout Example

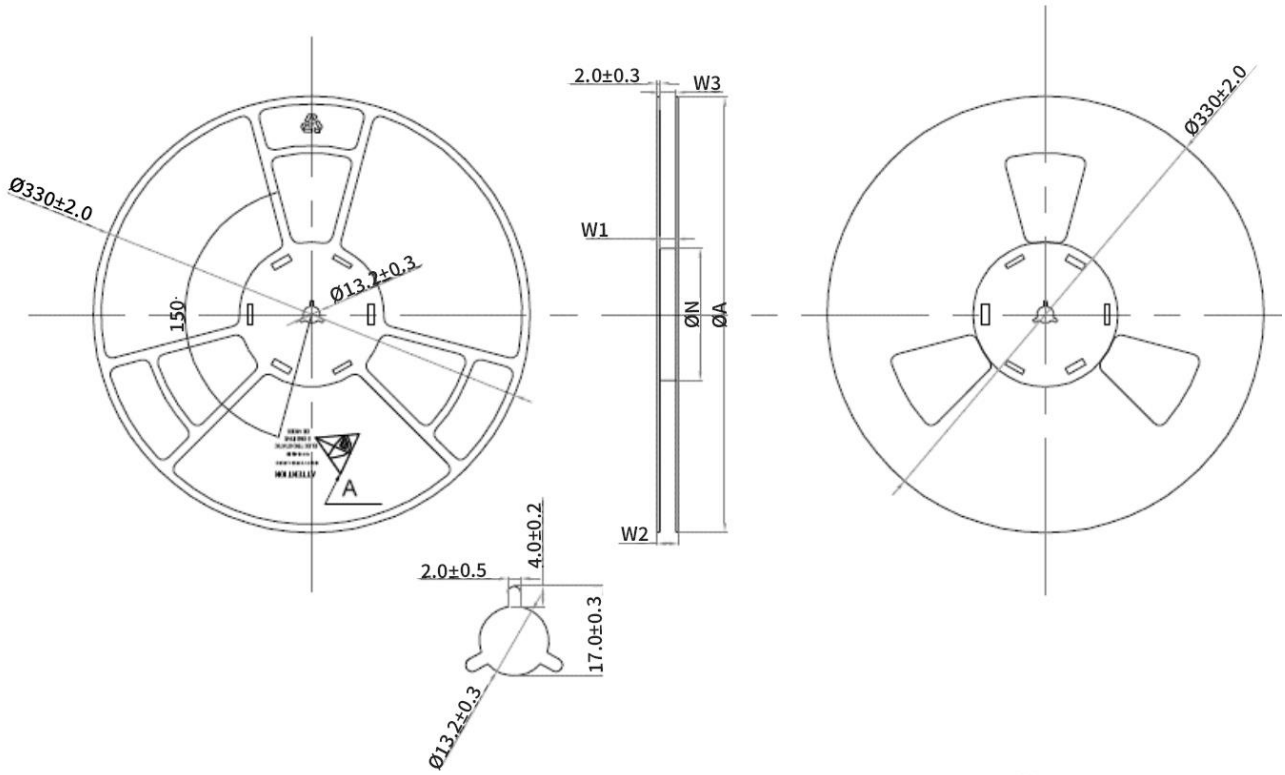
10. Order information

Part Number	*Pins*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*Package Qty*
NCA9548-DTSXR	24	-40 to 105℃	2	TSSOP24	TSSOP	3000

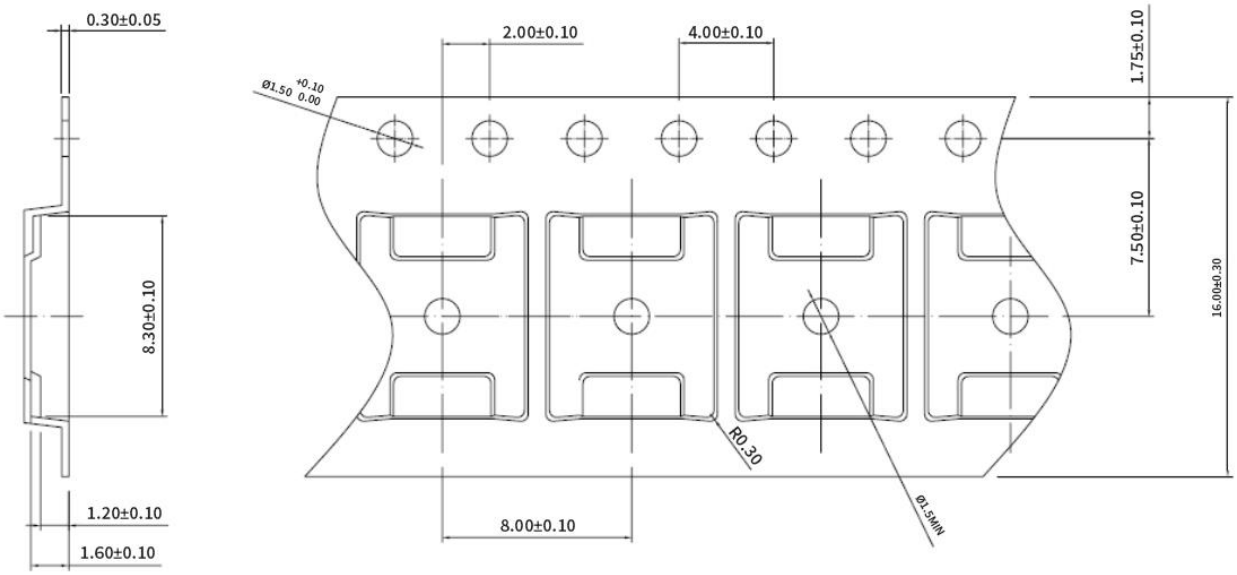
11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA9548	Click here	Click here	Click here	Click here

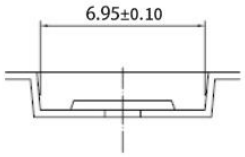
12. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	∅A	∅N	W1(+2/0)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4 (B)	11.9/15.4
16MM	330±2.0	100±1.0	16.4	22.4 (B)	15.9/19.4
24MM	330±2.0	100±1.0	24.4	30.4 (B)	23.9~27.4



NOTES:
1.10 sprocket hole pitch cumulative tolerance±0.2
2.Camber not to exceed imm in 250mm.
3.Material:Black conductive Polystyrene.
4.Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5.Ko measured from a plane on the inside bottom of the pocket to the top suface of the carrier.
6.Pocket postion ralative to sprocket hole measured as true postion of pocket,not pocket hole.
7.Pocket center and pocket hole center must be same postion.



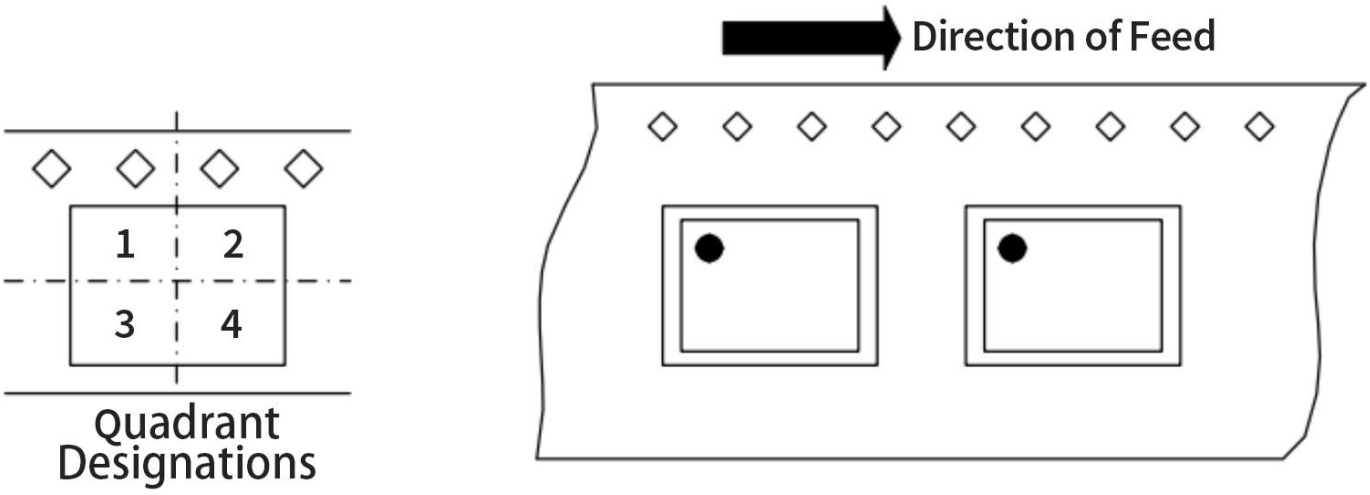


Figure 12.1 Tape and Reel Information of TSSOP24

13. Revision History

Revision	*Description*	*Date*
1.0	Initial version	2021/3/10
1.1	Change Storage Temperature. Update Package Board Layout Example	2022/4/28

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