

### Product Overview

The NCA9617A is a BiCMOS dual bidirectional buffer intended for I2C-bus and SMBus systems. It can provide bidirectional voltage-level translation (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (2.2V-5.5V) in mixed-mode applications. This device enables I2C and similar bus systems to be extended, without degradation of performance even during level shifting.

The NCA9617A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I2C-bus, allowing two buses of 550-pF or greater bus capacitance to be connected in an I2C application.

This device can also be used to isolate two halves of a bus for voltage and capacitance.

### Key Features

- Two-Channel Bidirectional I2C Buffer
- Support for Standard Mode, Fast Mode (400 kHz), and Fast Mode+ (1 MHz) I2C Operation
- Operating Supply Voltage Range of 0.8 V to 5.5 V on A-Side
- Operating Supply Voltage Range of 2.2 V to 5.5 V on B-Side
- Voltage-Level Translation From 0.8 V to 5.5 V and 2.2 V to 5.5 V
- Active-High Repeater-Enable Input
- Open-Drain I2C I/O
- 5.5-V Tolerant I2C and Enable Input Support
- Mixed-Mode Signal Operation
- Lockup-Free Operation

- Support for Clock Stretching and Multiple Master
- Arbitration Across The Device
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5500-V Human-Body Model (A114-A)
  - 1500-V Charged-Device Model (C101)

### Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products With Many I<sup>2</sup>C Slaves and/or Long PCB

### Device Information

Part Number	Package	Body Size
NCA9617A-DMSR	MSOP8	3.00mm*3.00mm

### Functional Block Diagrams

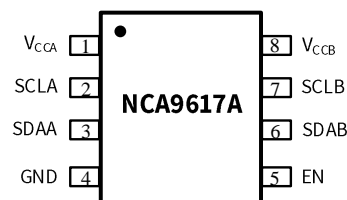


Figure 1 NCA9617A Block Diagram

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## 1. Pin Configuration and Functions

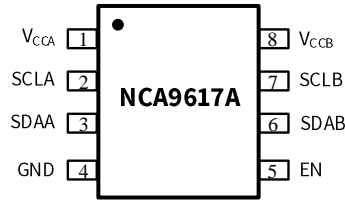


Figure 1. 1 NCA9617A Package

Table 1. 1 Pin Description

Symbol	Pin	Description
V <sub>CCA</sub>	1	Port A supply voltage (0.8V to 5.5V)
SCLA	2	Serial clock port A bus
SDAA	3	Serial data port A bus
GND	4	Supply ground
EN	5	Active HIGH repeater enable input
SDAB	6	Serial data port B bus
SCLB	7	Serial clock port B bus
V <sub>CCB</sub>	8	Port B supply voltage (2.2V to 5.5V)

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage	V <sub>CCA</sub>	-0.5		7	V	
	V <sub>CCB</sub>	-0.5		7	V	
Input/output Voltage	V <sub>I</sub> /V <sub>O</sub>	-0.5		7	V	EN, SCLx, SDAx
Input clamp current	I <sub>IK</sub>			-50	mA	V <sub>I</sub> <0V
Output clamp current	I <sub>OK</sub>			-50	mA	V <sub>O</sub> <0V
Continuous output current	I <sub>O</sub>			±50	mA	
Continuous current through V <sub>CC</sub> or GND	I <sub>CC</sub>			±100	mA	
Operating free-air temperature	T <sub>A</sub>	-40		105	°C	
Storage Temperature	T <sub>stg</sub>	-65		150	°C	
Electrostatic discharge	HBM			±5500	V	
	CDM			±1500	V	

### 3. Recommended Operating Conditions

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Supply voltage, A-side bus	$V_{CCA}$	0.8		$V_{CCB}$	V
Supply voltage, B-side bus	$V_{CCB}$	2.2		5.5	V
Low-level output current	$I_{OLA}$			13	mA
Low-level output current	$I_{OLB}$	0.1		13	mA

### 4. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>MSOP-8</i>	<i>Unit</i>
Junction-to-ambient thermal resistance	$\theta_{JA}$	171.8	$^{\circ}\text{C}/\text{W}$
Junction-to-case(top) thermal resistance	$\theta_{JC (top)}$	61.2	$^{\circ}\text{C}/\text{W}$
Junction-to-board thermal resistance	$\theta_{JB}$	93.6	$^{\circ}\text{C}/\text{W}$

## 5. Specifications

### 5.1. Electrical Characteristics

( $V_{CCA}=0.8V\sim 5.5V$ ,  $V_{CCB}=2.2V\sim 5.5V$ ,  $T_A=-40^{\circ}C$  to  $105^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{CCA} = 0.95V$ ,  $V_{CCB} = 2.5V$ ,  $T_A = 25^{\circ}C$ )

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
<b>Supplies</b>						
Supply voltage	$V_{CCA}^2$	0.8		5.5	V	
	$V_{CCB}$	2.2		5.5	V	
Supply current	$I_{CCA}$			8	$\mu A$	$V_{CCA} = 0.95V$
				50	$\mu A$	$V_{CCA} = 5.5V$
	$I_{CCB}$		1.4	2.5	mA	$V_{CCB} = 5.5V$ , $SDAn=SCLn=V_{CCn}$
			1.4	2.9	mA	$V_{CCB}=5.5V$ , $SDAA$ and $SCLA=GND$ , $SDAB$ and $SCLB$ pull up to $V_{CCB}$ with resistors
	1.7	2.9	mA	$V_{CCB}=5.5V$ , $SDAB$ and $SCLB=GND$ , $SDAA$ and $SCLA$ pull up to $V_{CCA}$ with resistors		
<b>Input and Output SDAA and SCLA</b>						
LOW-level input voltage	$V_{IL}^3$	-0.5		0.3* $V_{CCA}^4$	V	
HIGH-level input voltage	$V_{IH}$	0.7* $V_{CCA}$		5.5	V	
Input clamping voltage	$V_{IK}$	-1.2		-0.3	V	$I_i=-18mA$ ; $EN=LOW$
LOW-level output voltage	$V_{OL}$		0.1	0.2	V	$I_{oL}=13mA$ ; $V_{CCB}=2.2V$
Input leakage current	$I_{LI}$	-1		+1	$\mu A$	$V_i = 5.5V$
LOW-level input current	$I_{IL}$	-1		+1	$\mu A$	$V_i = 0V$
Input/output capacitance	$C_{io}^8$		7	10	pF	$V_i = 3V$ or $0V$ ; $V_{CCB}=3.3V$ ; $EN=LOW$
			7	10	pF	$V_i = 3V$ or $0V$ ; $V_{CCA}=0V$ ;
<b>Input and Output SDAB and SCLB</b>						
LOW-level input voltage	$V_{IL}^5$	-0.5		0.4	V	
HIGH-level input voltage	$V_{IH}$	0.7* $V_{CCB}$		5.5	V	

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Input clamping voltage	$V_{IK}$	-1.2		-0.3	V	$I_I = -18\text{mA}$ ; EN=LOW
LOW-level output voltage	$V_{OL}$	0.45			V	$I_{OL} = 150\mu\text{A}$ ; $V_{CCB} = 2.2\text{V}^5$
			0.56	0.62	V	$I_{OL} = 13\text{mA}$ ; $V_{CCB} = 2.2\text{V}^6$
Difference between LOW-level output and LOW-level input voltage	$V_{OL} - V_{IL}$	60	90	160	mV	$V_{OL}$ at $I_{OL} = 1\text{mA}$ ; guaranteed by design
Input leakage current	$I_{LI}$	-1		+1	$\mu\text{A}$	$V_I = 5.5\text{V}$
LOW-level input current	$I_{IL}$	-1		+1	$\mu\text{A}$	$V_I = 0\text{V}$ ; EN=LOW
Input/output capacitance	$C_{io}^8$		7	10	pF	$V_I = 3\text{V}$ or $0\text{V}$ ; $V_{CCB} = 3.3\text{V}$ ; EN=LOW
			7	10	pF	$V_I = 3\text{V}$ or $0\text{V}$ ; $V_{CCB} = 0\text{V}$ ;
<b>Enable</b>						
LOW-level input voltage	$V_{IL}$	-0.5		$0.3^* V_{CCB}$	V	
HIGH-level input voltage	$V_{IH}$	$0.7^* V_{CCB}$		5.5	V	
Input leakage current	$I_{LI}$	-1		+1	$\mu\text{A}$	
LOW-level input current	$I_{IL}$	-18	-7	-4	$\mu\text{A}$	$V_I = 0\text{V}$ , $V_{CCB} = 2.2\text{V}$
Input capacitance	$C_I^8$		6	7	pF	$V_I = V_{CCB}$

- $V_{CCA}$  may be as high as 5.5V for overvoltage tolerance but  $0.4V_{CCA} + 0.8V \leq V_{CCB}$  for the channels to be enabled and functional normally.
- For part to function,  $0.4V_{CCA}$  must be equal or less than  $V_{CCB} - 0.8V$ . The voltage on the A port can still be up to 5.5V without damage to the pins.
- $V_{IL}$  for port A with envelope noise must be below  $0.3V_{CCA}$  for stable performance.
- When  $V_{CCA}$  is less than 1V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the  $V_{IL}$  present at the NCA9617AA-side input and the  $0.3V_{CCA}$  input threshold.
- Pull-up should result in  $I_{OL} \geq 150\mu\text{A}$ .
- Guaranteed by design and characterization.
- Power supply decoupling capacitors need to be present for both  $V_{CCA}$  and  $V_{CCB}$  and the  $0.1\mu\text{F}$  decoupling for  $V_{CCB}$  needs to be located near the  $V_{CCB}$  pin.
- Not tested in production; guaranteed by design.

### 5.2. Dynamic Characteristics

( $V_{CCA}=0.8V\sim 5.5V$ ,  $V_{CCB}=2.2V\sim 5.5V$ ,  $T_A=-40^{\circ}C$  to  $105^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{CCA} = 0.95V$ ,  $V_{CCB} = 2.5V$ ,  $T_A=25^{\circ}C$ )<sup>2,3</sup>

Parameter	Symbol	min	Typ <sup>4</sup>	Max	Unit	Conditions
Propagation delay	$t_{PLH1}$	-103	-23	-9	ns	Port B to port A; see Figure 5. 3
	$t_{PLH2}$	50	84	120	ns	Port B to port A; see Figure 5. 3 <sup>5</sup>
	$t_{PLH3}$	40	77	200	ns	Port A to port B; see Figure 5. 2
	$t_{PHL1}$	15	37	120	ns	Port B to port A; see Figure 5. 1
	$t_{PHL2}$	10	53	110	ns	Port A to port B; see Figure 5. 2 <sup>7</sup>
LOW to HIGH output transition time	$t_{TLH}$		88		ns	port A; see Figure 5. 1 <sup>6</sup>
			85		ns	port B; see Figure 5. 2
Failing slew rate	$SR_f^9$	0.022	0.037	0.11	V/ns	port A; $0.7V_{CCA}$ to $0.3V_{CCA}$
		0.029	0.056	0.09	V/ns	port B; $0.7V_{CCB}$ to $0.3V_{CCB}$
Enable time	$t_{en}$			100	ns	Quiescent $-0.3V$ ; enable high to enable; see Figure 5. 4 <sup>8</sup>
Disable time	$t_{dis}$			100	ns	Quiescent $+0.3V$ ; enable LOW to disable; see Figure 5. 4

- $0.4V_{CCA} + 0.8V \leq V_{CCB}$  for the channels to be enabled and function normally.
- Times are specified with loads of  $1.35k\Omega$  pull-up resistance and  $50\text{ pF}$  load capacitance on port A and port B, and a falling edge slew rate of  $0.05V/ns$  input signals.
- Pull-up voltages are  $V_{CCA}$  on port A and  $V_{CCB}$  on port B.
- Typical values were measured with  $V_{CCA} = 0.95V$ ,  $V_{CCB} = 2.5V$  at  $T_A = 25^{\circ}C$ , unless otherwise noted.
- The  $t_{PLH2}$  delay data from port B to port A is measured at  $0.45V$  on port B to  $0.5V_{CCA}$  on port A.
- The  $t_{TLH}$  of the bus is determined by the pull-up resistance ( $1.35k\Omega$ ) and the total capacitance ( $50pF$ ).
- The proportional delay data from port A to port B is measured at  $0.5V_{CCA}$  on port A to  $0.5V_{CCB}$  on port B.
- The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.
- Not tested in production; guaranteed by design.

### 5.3. Parameter Measurement Information

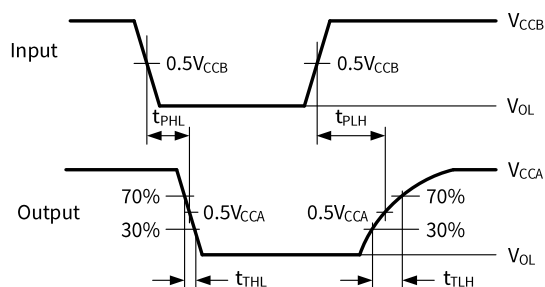


Figure 5. 1 Propagation delay and transition times port B to port A

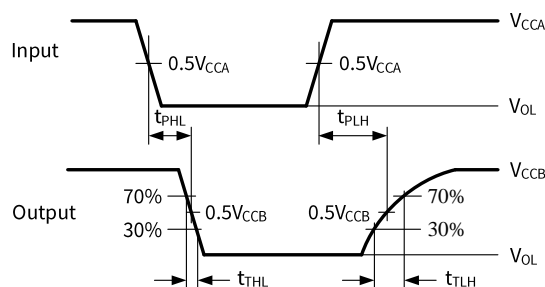


Figure 5. 2 Propagation delay and transition times port A to port B

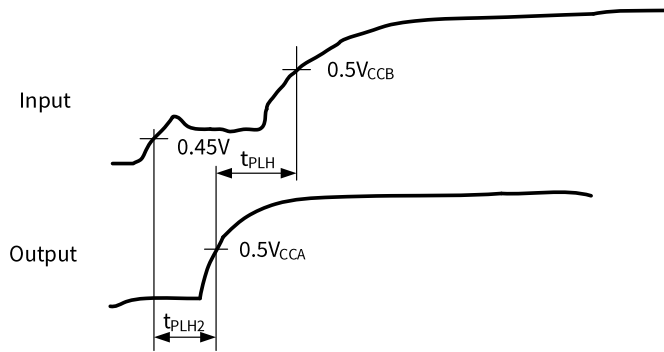


Figure 5.3 Propagation delay

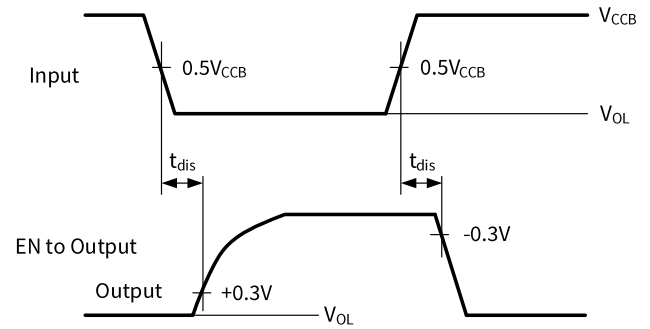


Figure 5.4 Enable and disable time

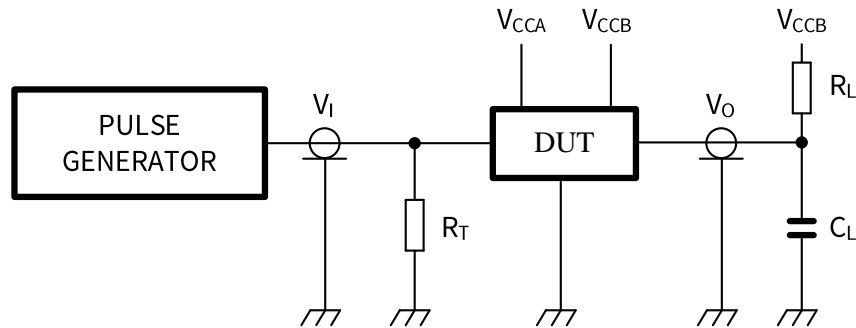


Figure 5.5 Test circuitry for switching times

Definitions test circuit:

$R_L$  = Load resistance; 1.35k $\Omega$  on port A and port B.

$C_L$  = Load capacitance includes jig and probe capacitance; 50pF.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.



## 6. Detailed Description

### 6.1. Overview

The NCA9617A enables I<sup>2</sup>C-bus or SMBus translation down to  $V_{CCA}$  as low as 0.8V without degradation of system performance. The NCA9617A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8V) and a 2.5V, 3.3V or 5V I<sup>2</sup>C-bus or SMBus systems. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered ( $V_{CCB}$  and/or  $V_{CCA} = 0V$ ). The NCA9617A includes a power-up circuit that keeps the output drivers turned off until  $V_{CCB}$  is above 2.2V and until after the internal reference circuits have settled  $\sim 400\ \mu s$ , and the  $V_{CCA}$  is above 0.8V.  $V_{CCB}$  and  $V_{CCA}$  can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port A (below  $0.3V_{CCA}$ ) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55V. When port A rises above  $0.3V_{CCA}$ , the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4V, the port A driver is turned on and port A pulls down to  $\sim 0V$ . The port A pull-down is not enabled unless the port B voltage goes below 0.4V. If the port B low voltage goes below 0.4V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55V until port A rises above  $0.3V_{CCA}$ , then port B will continue to rise being pulled up by the external pull-up resistor. The  $V_{CCA}$  is only used to provide the  $0.35V_{CCA}$  reference to the port A input comparators and for the power good detect circuit. The NCA9617A includes a  $V_{CCA}$  overvoltage disable that turns the channel off if  $0.4V_{CCA} + 0.8V > V_{CCB}$ . The NCA9617A logic and all I/Os are powered by the  $V_{CCB}$  pin.

### 6.2. Functional Block Diagram

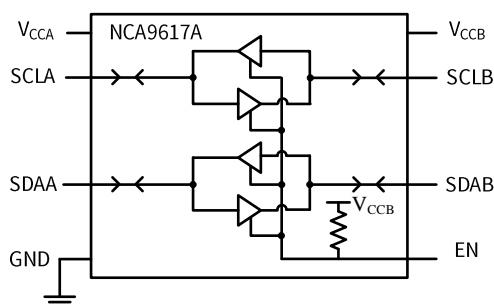


Figure 6. 1 NCA9617A Functional block

### 6.3. Enable

The EN pin is active HIGH with thresholds referenced to  $V_{CCB}$  and an internal pull-up to  $V_{CCB}$  that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus parts being enabled. The enable does not switch the internal reference circuits so the  $\sim 400\ \mu s$  delay is only seen when  $V_{CCB}$  comes up.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

### 6.4. I<sup>2</sup>C-Bus System

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I<sup>2</sup>C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I<sup>2</sup>C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I<sup>2</sup>C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30mA at 5V drive strength, then lower value pull-up resistors can be used. The B-side RC should not be less than 67.5ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

## 7. Application and Implementation

A typical application is shown in Figure 7. 1. In this example, the system master is running on a 3.3V I<sup>2</sup>C-bus while the slave is connected to a 1.2V bus. Both buses run at 1000kHz. Master devices can be placed on either bus.

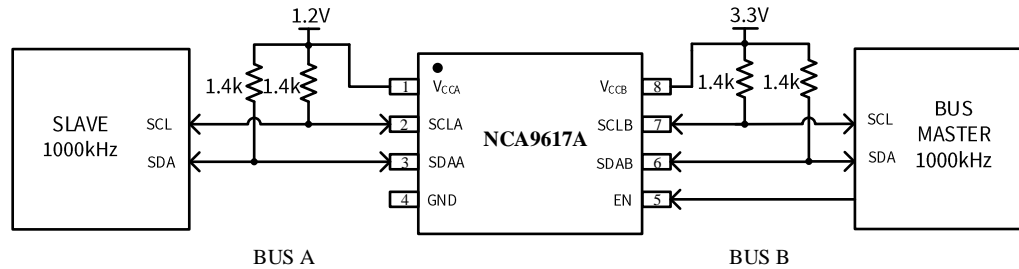


Figure 7. 1 NCA9617A Typical application

The NCA9617A is 5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5V bus voltages and 2.2V to 5.5V bus voltages. When port A of the NCA9617A is pulled LOW by a driver on the I<sup>2</sup>C-bus, a comparator detects the falling edge when it goes below  $0.3V_{CCA}$  and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5V. When port B of the NCA9617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 7. 5 and Figure 7. 6. If the bus master in Figure 7. 1 were to write to the slave through the NCA9617A, waveforms shown in Figure 7.5 would be observed on the A bus. This looks like a normal I<sup>2</sup>C-bus transmission except that the HIGH level may be as low as 0.8V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The internal comparator requires that  $0.4V_{CCA}$  be less than or equal to  $V_{CCB}-0.8V$  for the device to operate. Since A port is 5V tolerant, the  $V_{CCA}$  can be lowered to support device spectrum while still supporting 5V signals on the A port. On the B bus side of the NCA9617A, the clock and data lines would have a positive offset from ground equal to the  $V_{OL}$  of the NCA9617A. After the eighth clock pulse, the data line will be pulled to the  $V_{OL}$  of the slave device which is very close to ground in this example.

At the end of the acknowledge, the level rises only to the LOW-level set by the driver in the NCA9617A for a short delay while the A bus side rises above  $0.3V_{CCA}$  then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW-level on the B bus side at the input of the NCA9617A ( $V_{IL}$ ) be at or below 0.4V to be recognized by the NCA9617A and then transmitted to the A bus side.

Multiple NCA9617A port A sides can be connected in a star configuration (Figure 7. 2), allowing all nodes to communicate with each other. Multiple NCA9617As can be connected in series (Figure 7. 3) as long as port A is connected to port B. I<sup>2</sup>C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

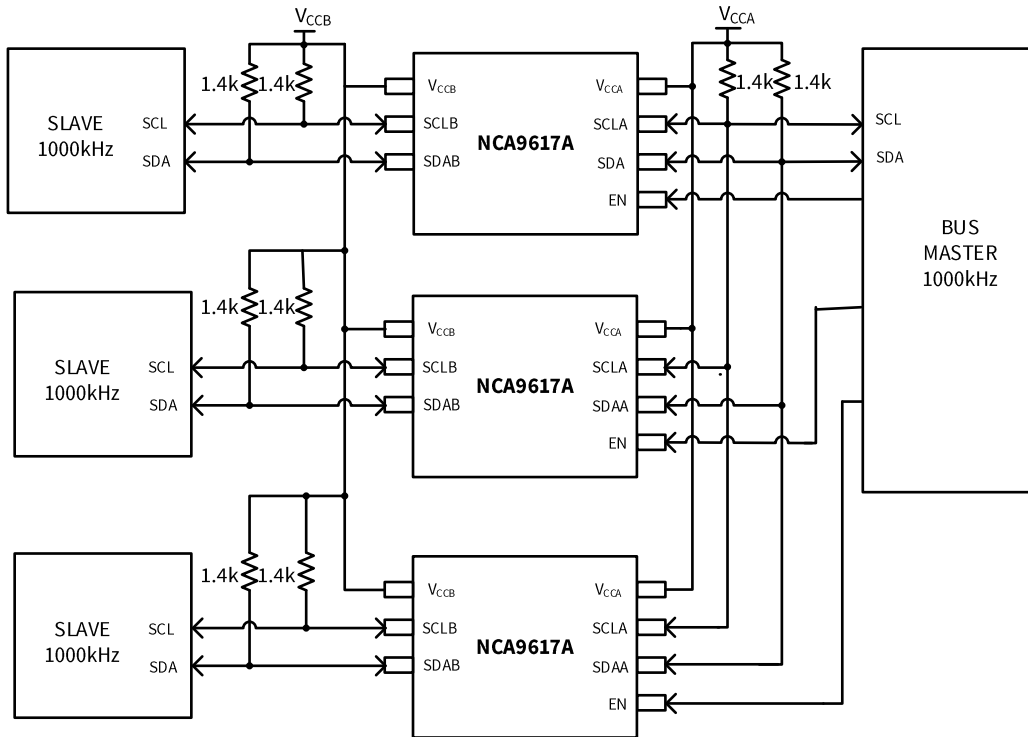
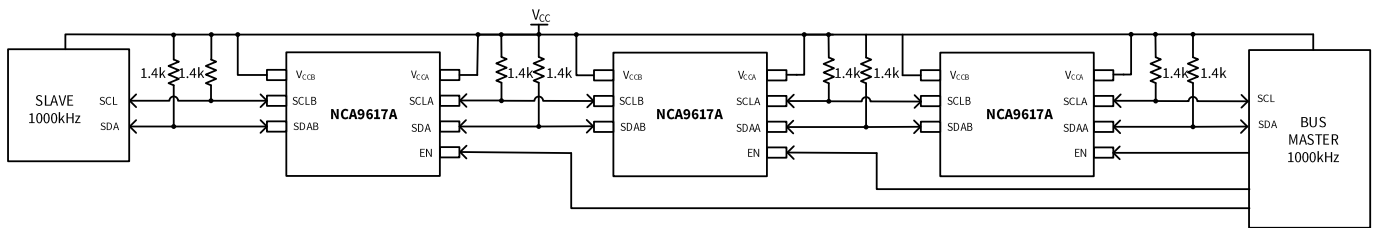
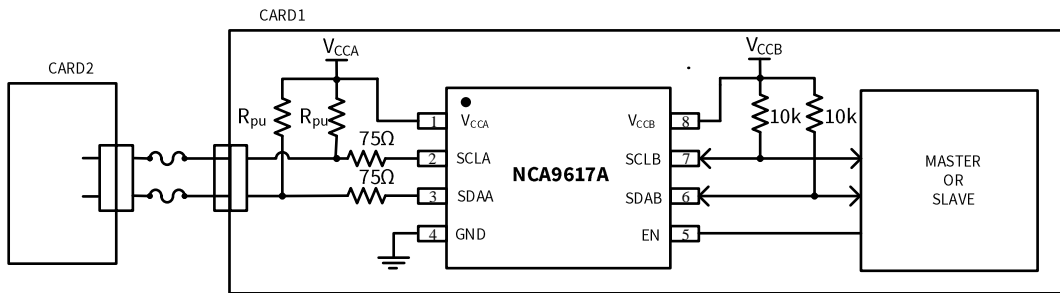


Figure 7.2 Typical star application



Decoupling capacitors not shown for simplicity. But they are required. It is especially important that the decoupling for the NCA9617A  $V_{CCB}$  be close to the  $V_{CCB}$  pin

Figure 7.3 Typical series application



Decoupling capacitors not shown for simplicity. But they are required. It is especially important that the decoupling for the NCA9617A  $V_{CCB}$  be close to the  $V_{CCB}$  pin

Figure 7.4 Typical application of NCA9617A driving a short cable

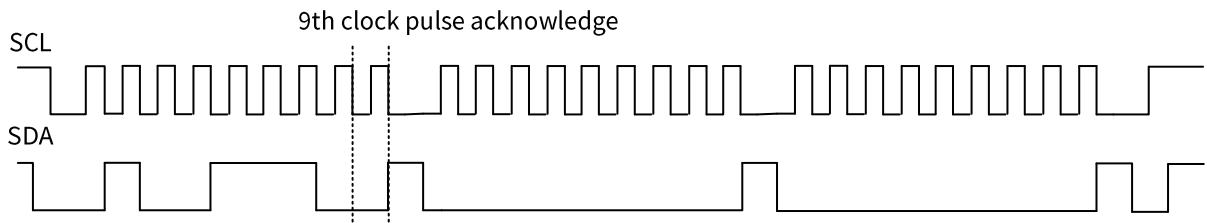


Figure 7.5 Bus A (0.8V to 5.5V) waveform

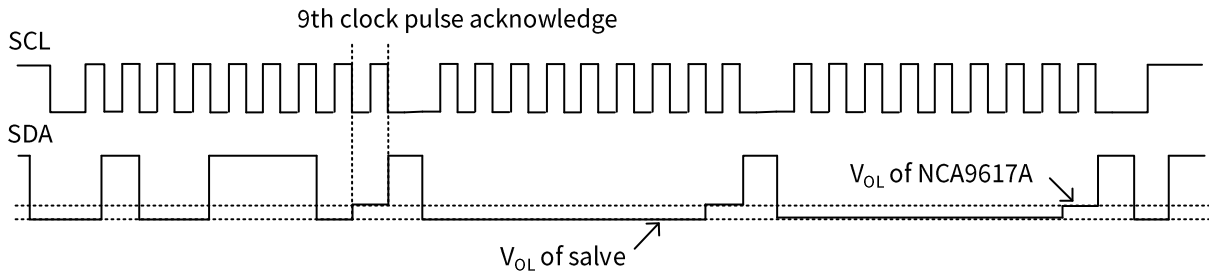


Figure 7.6 Bus B (2.2V to 5.5V) waveform

## 8. Layout

### 8.1. Layout Guidelines

The recommended decoupling capacitors should be placed as close to the  $V_{CCA}$  and  $V_{CCB}$  pins of the NCA9617A as possible.

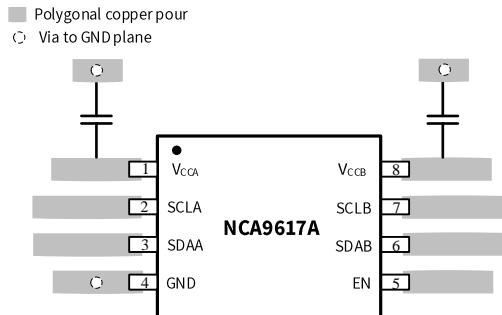
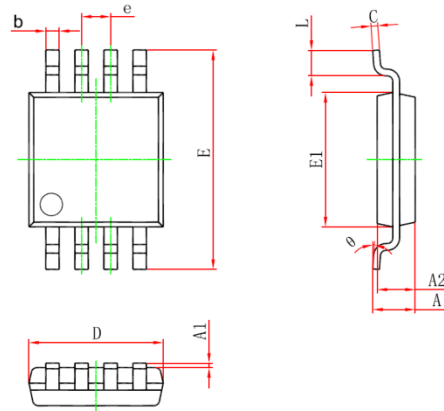


Figure 8.1 Recommended PCB layout

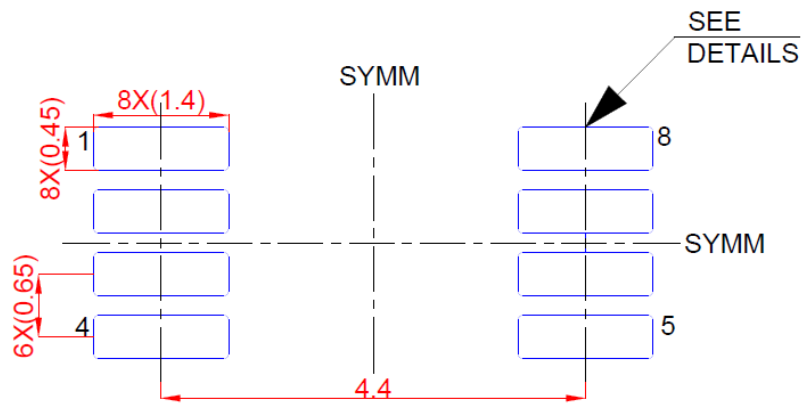
### 9. Package Information



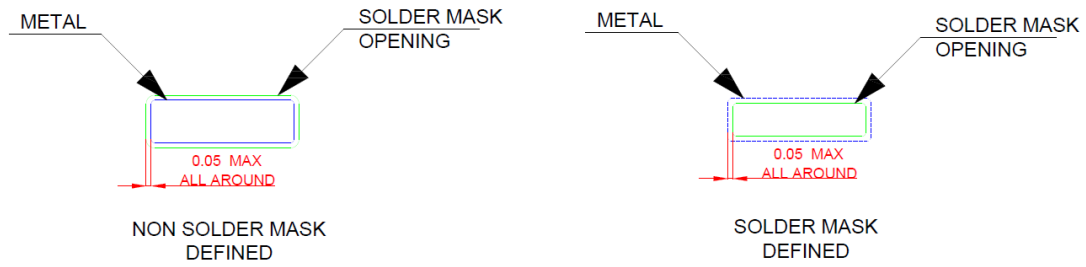
NOTES:  
ALL DIMENSIONS MEET JEDEC STANDARD MO-187 AA

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	1.100	---	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Figure 9.1 Package outline for MSOP8



LAND PATTERN EXAMPLE (mm)



SOLDER MASK DETAILS

Figure 9. 2 MSOP8 Package Board Layout Example

### 10. Order information

Part Number	Pins	Temperature	MSL	Package Type	Package Drawing	SPQ
NCA9617A-DMSR	8	-40 to 105°C	3	MSOP	MSOP	4000

### 11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NCA9617A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12. Tape and Reel Information

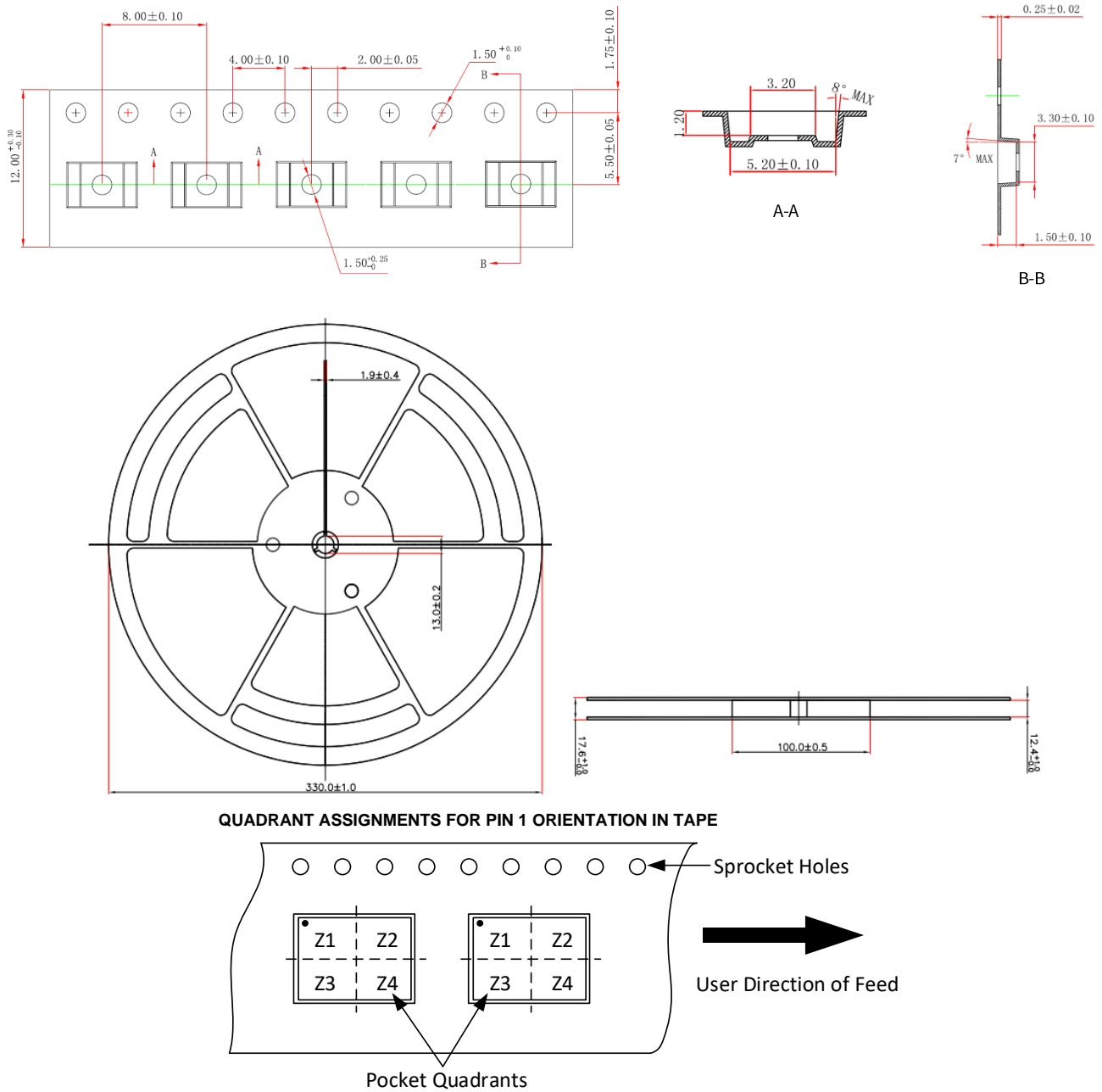


Figure 12. 1 Tape and Reel Information of MSOP8

### 13. Revision history

Revision	Description	Date
1.0	Initial version	2022/12/10

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