NOVOSENSE
纳芯微电子

NSi3190

NSI3190: Isolated Error Amplifier

Datasheet (EN) 1.3

Product Overview

The NSI3190 is a high reliability isolated error amplifier based on NOVOSENSE capacitive isolation technology. The NSI3190 is ideal for linear feedback power supplies. The primary side controllers of the NSI3190 enable improvements in transient response, power density, and stability as compared to commonly used optocoupler and shunt regulator solutions.

The output of NSI3190 can not only support voltage output, but also current output that is compatible to optocoupler. The current transfer coefficient can be set by external resistor between EAOUT2 and VDD1 or VREG1

Key Features

- 0.5% Initial Accuracy
- Up to 3000VRMS Insulation Voltage
- Bandwidth: 400kHz
- Power Supply Voltage:
- VDD1: 4V to 20V
- VDD2: 4V to 20V
- Reference Voltage 1.225V
- High CMTI: 100kV/us
- Support Voltage Output and Current Output
- Low Power Consumption
- Operation Temperature: -40℃~125℃
- Junction Temperature: 150℃
- RoHS-Compliant Packages: SSOP-16

Safety Regulatory Approvals

- UL recognition: up to 3kVRMS for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval
- DIN VDE V 0884-11:2017-01

Applications

- DOSA compatible modules
- Inverters
- UPS
- Voltage monitors
- Power System

Device Information

Part Number	*Package Type*	*Body Size*
NSI3190-DSSR	SSOP16	5.0mm × 4.00mm

Functional Block Diagrams

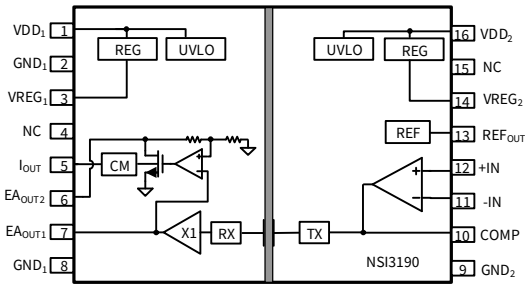

Figure 1. NSi3190 Block Diagram

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1. Pin Configuration and Functions

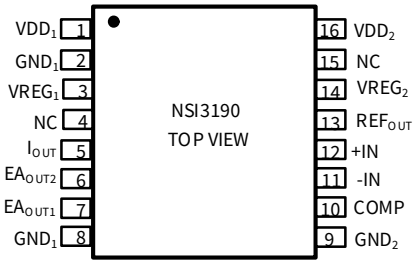


Figure 1.1 NSi3190 Package

Table 1.1 NSi3190 Pin Configuration and Description

NSI3190 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power Supply for Isolator Side 1(4V to 20V).
2	GND1	Ground 1, the ground reference for Isolator Side 1
3	$VREG_1$	Side1 Internal Supply Voltage, 3.3V. Need 1.0uF bypass capacitor.
4	NC	The NC Pin must be pull high or floating
5	I_{OUT}	Isolated Output Current.
6	EA_{OUT2}	Isolated Output Voltage 2, Open Drain output.
7	EA_{OUT1}	Isolated Output Voltage 1.
8	GND1	Ground 1, the ground reference for Isolator Side 1
9	GND2	Ground 2, the ground reference for Isolator Side 2
10	COMP	Output of the Op Amp. A loop compensation network can be connected between the COMP pin and the -IN pin.
11	-IN	Inverting Op Amp Input. Pin 11 is the connection for the power supply setpoint and compensation network.
12	+IN	Noninverting Op Amp Input. Pin 12 can be used as a reference input.
13	REF_{OUT}	Reference Output Voltage for Side 2. The maximum capacitance for this pin (C_{REFOUT}) must not exceed 15pF.
14	$VREG_2$	Side2 Internal Regulator Output, Output 3.3V, Need 1.0uF bypass capacitor
15	NC	The NC pin need to be connected to ground or left floating.
16	VDD2	Power Supply for Isolator Side 2 (4V to 20V).

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		24	V	
Maximum Input Voltage	+IN, -IN	-0.4		3.6	V	
Maximum Output Voltage	EAOUT2	-0.4		6.5	V	EAOUT2 can't be pulled high to above 6.5V
Common-Mode Transients	CMTI	-100		+100	kV/us	
Output current per Output Pin	Io	-15		15	mA	
Maximum Surge Isolation Voltage	VIOSM			5	kV	
Operating Temperature	TOPR	-40		125	℃	
Storage Temperature	TSTG	-40		150	℃	
Electrostatic discharge	HBM			±2000	V	
	CDM			±500	V	

3. Thermal Information

Parameters	*Symbol*	*SSOP16*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}	84	°C/W

4. Specifications

4.1. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply						
Side1 Supply Voltage	VDD1	4		20	V	
Side2 Supply Voltage	VDD2	4		20	V	
Side1 Supply Current	IDD1		1.45	2.5	mA	EAOUT2 floating
Side2 Supply Current	IDD2		2.9	5	mA	
UVLO						
Positive Going Threshold	UVLOPOS		2.8	3	V	
Negative Going Threshold	UVLONEG	2.4	2.6		V	
EAOUT2 Impedance	ROUT		High-Z		Ω	VDD2 or VDD1 < UVLO threshold
Regulator Output						
Side1 Regulator Voltage	VREG1		3.3		V	
Side2 Regulator Voltage	VREG2		3.3		V	
Regulator Current	IREG	5			mA	
Reference	VREFOUT		1.225		V	CREFOUT=15pF
	IREFOUT			2	mA	
	IREFIN			0.2	mA	
Accuracy	ERRORINI		0.25	0.5	%	Ta=25℃, (1.225 V − EAOUT1)/1.225 V × 100%
	ERROR TOTAL		0.5	1	%	Ta=-40℃ to 125℃
OP AMP						
Offset Error	ERROROFF	-5	±2.5	5	mV	
Open-Loop Gain	GAINOPA		120		dB	
Bandwidth	BWOPA		10		MHz	
Input Common-Mode Range	VCOMM	0.35		1.5	V	

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Output Voltage Range	VCOMP	0.2		3	V	COMP pin
Input Bias Current	IBIAS		200		pA	
Common-Mode Rejection	CMR		72		dB	
Input Capacitance	CIN		2		pF	
OUTPUT CHARACTERISTICS						
EAOUT1 Output Gain	GAINOUT1		1		V/V	From COMP to EAOUT1
Output -3dB Bandwidth 1	BWOUTPUT	200	400		kHz	From COMP to EAOUT1
EAOUT1 Output Low Voltage	VEAOUTL1			0.4	V	IOUTPUT=-3mA
EAOUT1 Output High Voltage	VEAOUTH1	2.7	3		V	IOUTPUT=3mA
EAOUT1 Noise	NOISEOUT1		1.7m		Vrms	
IOUT Output Current	I IOUT	0		1	mA	Iout can be calculated by: $i(I_{OUT}) = (VDD_1 - EA_{OUT2})/Rx * 2\text{-}40\ uA$ *40uA is from Bias current inside the IC See Section 6.2 for more details. By setting suitable Rx the Iout can reach to 1.0mA
EAOUT2 Output Gain	GAINOUT2		2.6		V/V	From COMP to EAOUT2
EAOUT2 Output Low Voltage	VEAOUTL2			0.6	V	IOUTPUT=-1mA
EAOUT2 Output High Voltage	VEAOUTH2	VDD1-0.2	VDD1		V	VDD1=4.5V to 5.5V

[1] Parameter verified by design, not tested in production, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃

4.2. Typical Performance Characteristics

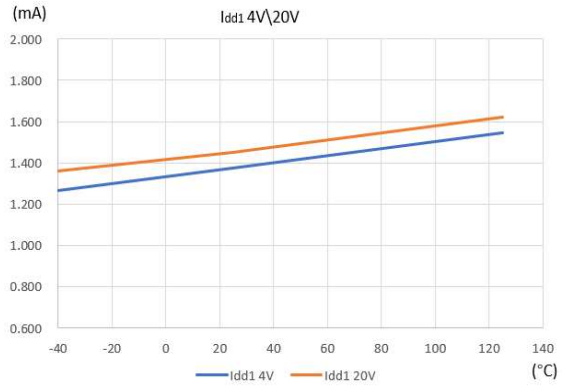


Figure 4.1 Typical Idd1 vs. T(℃)

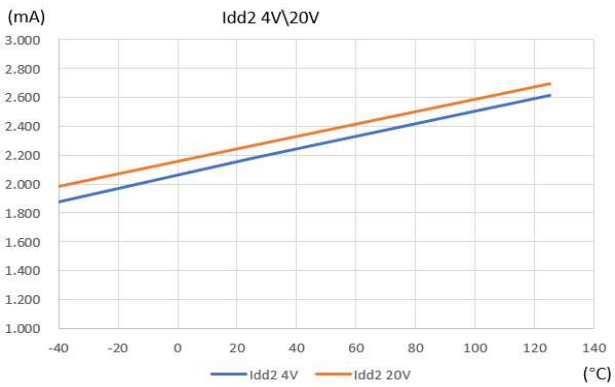


Figure 4.2 Typical Idd2 vs. T(℃)

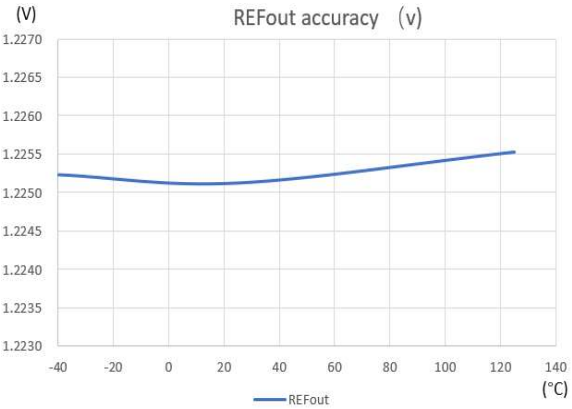


Figure 4.3 REFOUT accuracy(v) vs. T(℃)

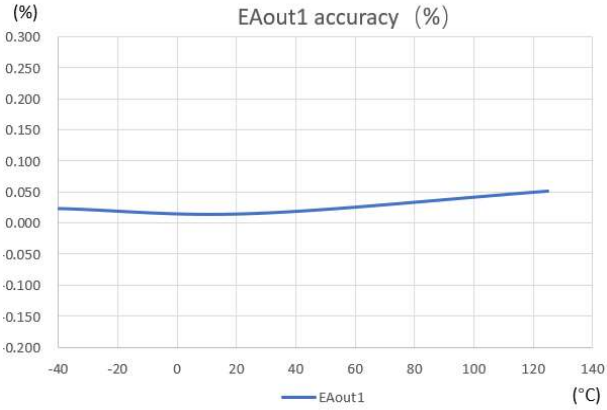


Figure 4.4 EAout1 accuracy (%) vs. T(℃)

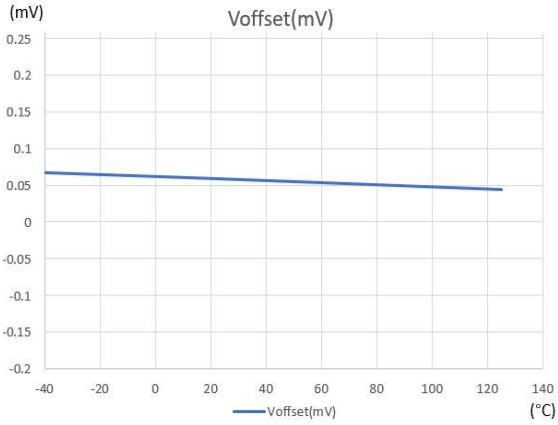


Figure 4.5 VOFFSET (mV) vs. T(℃)

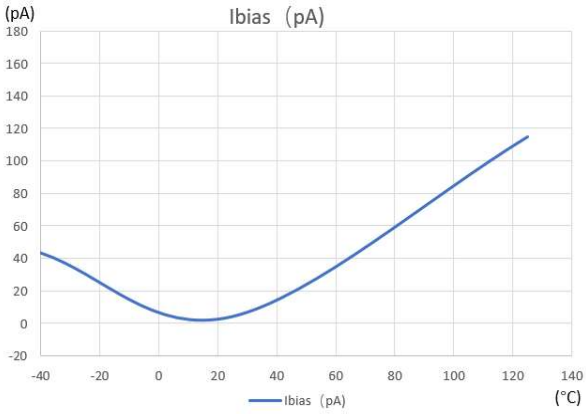


Figure 4.6. I_{BIAS} (pA) vs. T(℃)

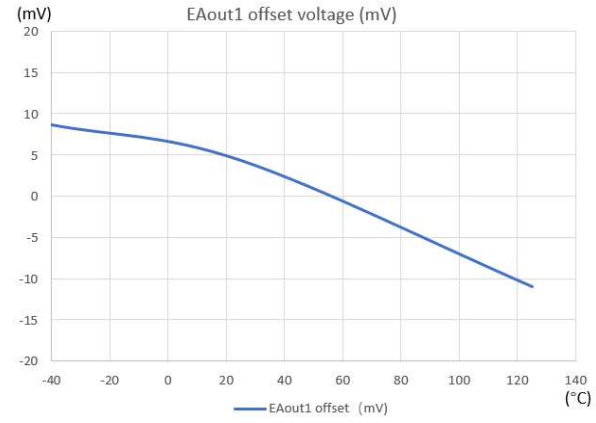


Figure 4.7 EA_{out1} offset (mV) vs. T(℃)

Figure 4.8 EA_{out2} offset (mV) vs. T(℃)

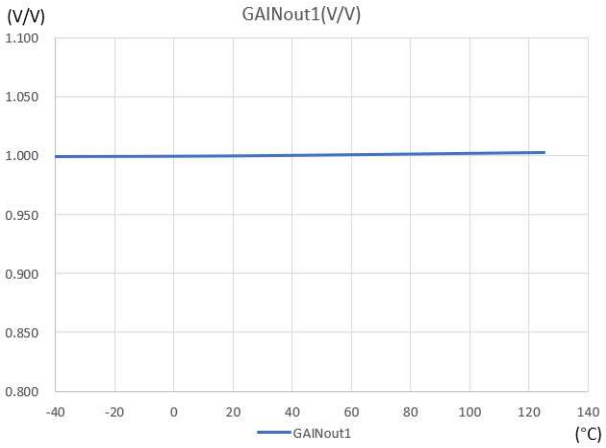


Figure 4.9 GAINOUT1 (V/V) vs. T(℃)

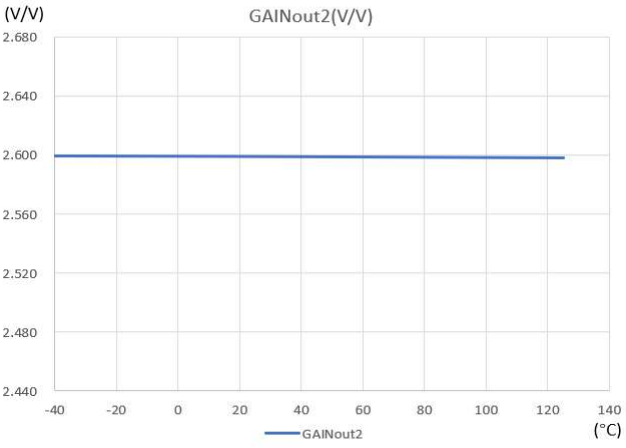


Figure 4.10 GAINOUT2 (V/V) vs. T(℃)

4.3. Parameter Measurement Information

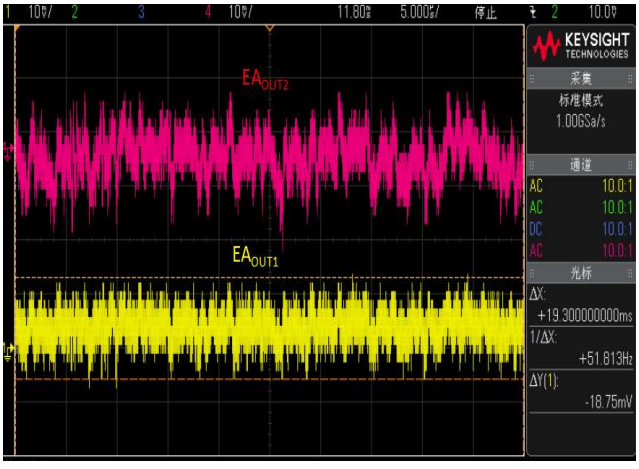


Figure 4.11 Ripple of EAOUT1

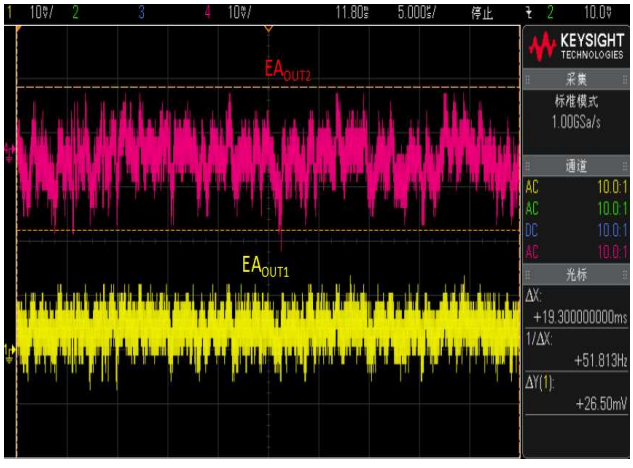


Figure 4.12 Ripple of EAOUT2

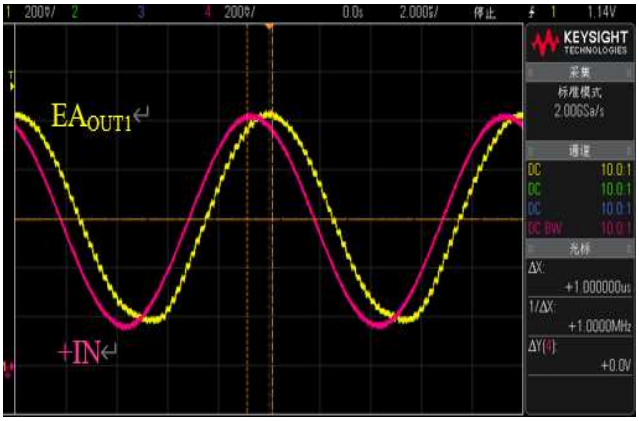


Figure 4.13 EAOUT1 follow with sinewave(overview)

Figure 4.14. EAOUT1 follow with sine wave (unfold)

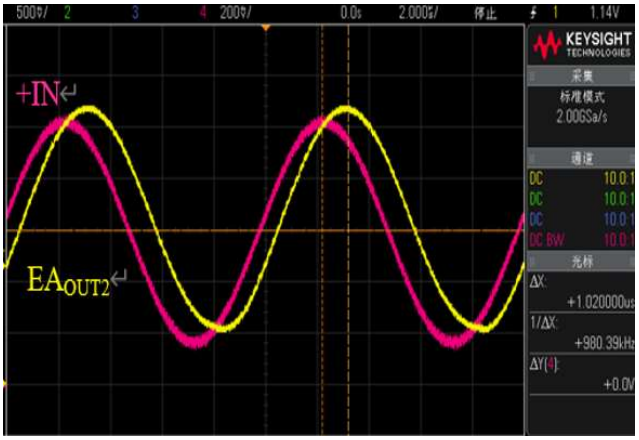


Figure 4.15 EAOUT2 follow with sine wave (overview)

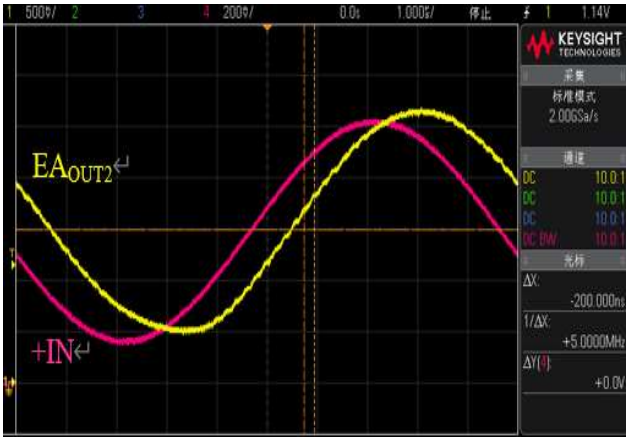


Figure 4.16 EAOUT2 follow with sine wave(unfold)

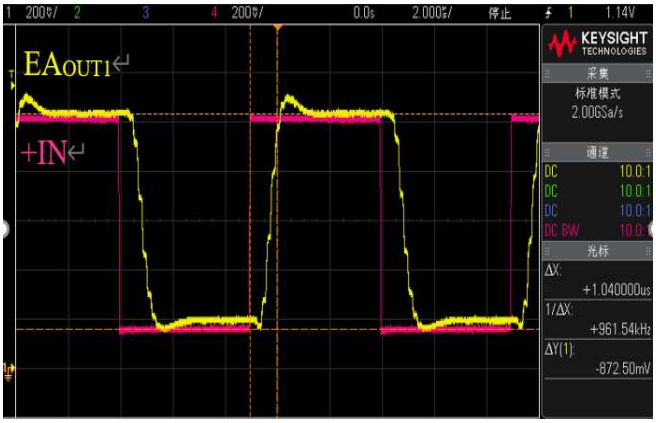


Figure 4.17 EA_{OUT1} follow with square wave

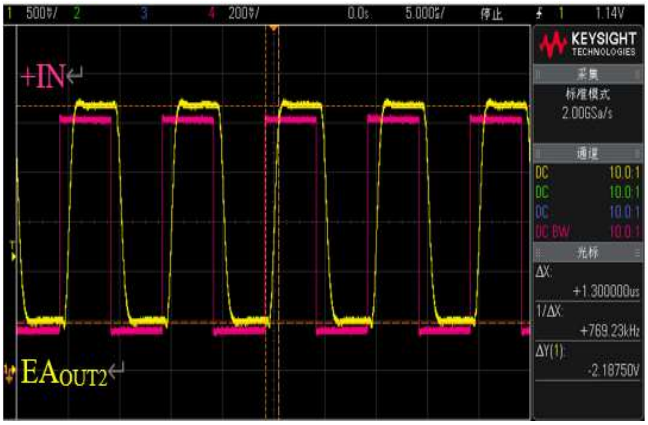


Figure 4.18 EA_{OUT2} follow with square wave

5. High Voltage Feature Description

5.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	3.9	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	3.9	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅱ		

5.2. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300Vrms			Ⅰ to Ⅲ	
For Rated Mains Voltage ≤ 400Vrms			Ⅰ to Ⅲ	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		VIORM	565	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1059	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	4242	Vpeak

Description	Test Condition	Symbol	Value	Unit
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, VTEST=VIOSM/1.3	VIOSM	5384	Vpeak
Isolation resistance	VIO =500V	RIO	>10^9	Ω
Input capacitance		CI	2	pF
Total Power Dissipation at 25℃		Ps		mW
Safety input, output, or supply current	θJA = 140 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	160	mA
	θJA = 84 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			mA
Case Temperature		Ts	150	℃

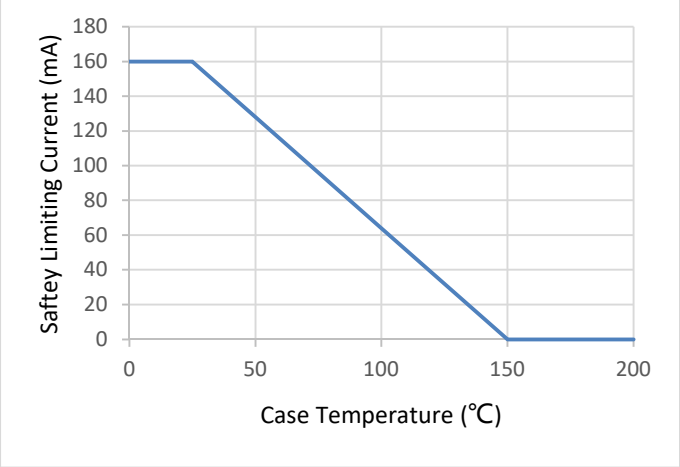


Figure 5.1 NSI3190 Thermal Derating Curve

Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

5.3. Regulatory Information

The NSi3190 is approved or pending approval by the organizations listed in table.

UL	CSA	VDE	CQC
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-11 (VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000Vrms Isolation voltage	400V_{RMS} basic insulation working voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation
Certificate No.E500602	Certificate No.E500602	Certificate No.40050121	CQC19001233128

[1] In accordance with UL 1577, each NSI3190 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-10, each NSI3190 is proof tested by applying an insulation test voltage ≥ 1059V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval

6. Function Description

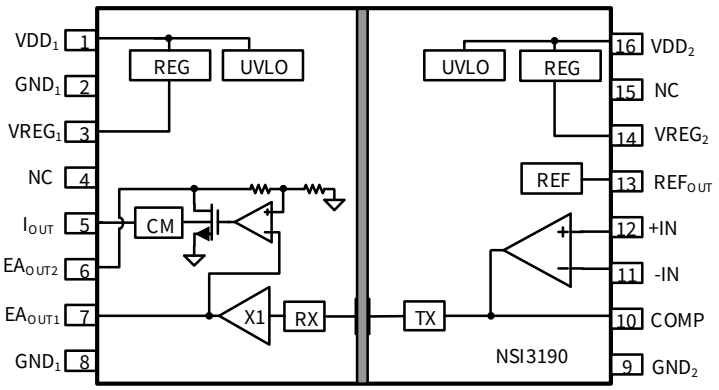


Figure 6.1 Function Block Diagram

6.1. Overview

The NSI3190 is a high reliability isolated error amplifier based on NOVOSENSE capacitive isolation technology. The NSI3190 is ideal for linear feedback power supplies. The primary side controllers of the NSI3190 enable improvements in transient response, power density, and stability as compared to commonly used optocoupler and shunt regulator solutions.

6.2. Current output

NSI3190 could provide current output so it can be used to directly replace the optocoupler. An external resistor Rx between pin VDD_1 and EA_{OUT2} is used to set the feedback current transfer coefficient. The current through I_{OUT} can be described as equation (1),

$$i(I_{\mathrm{OUT}}) = (VDD_1 - EA_{OUT}\ )/Rx * 2 - 40uA \quad (1)$$

The equation (1) could be used to set the Rx value according to the maximum I_{OUT} needed for the PWM controller. For instance, if I_{OUT_MAX} =1 mA, VDD_1=5V, EA_{OUT2_MIN}=0.3 V, the Rx should be no more than 9.4K ohm.

Equation (2) gives the accurate small signal transconductance from EA_{OUT2} to i(I_{OUT}), where C is the total parasitic cap of M_1 and M_2 which is about 10pF, and g_{m1} is the transconductance of M_1.

$$g_{m\_out} = \mathrm{i(Iout)}/v(EA_{OUT2}) = 2/Rx/(1 + s * Rx * C) \quad (2)$$

The gain of g_m can be approximately equal to 2/Rx for good linearity. The pole is located at 1/(2*π*Rx*C) which is larger than 1MHz.

7. Application Note

7.1. Typical application circuit for I_{out} output

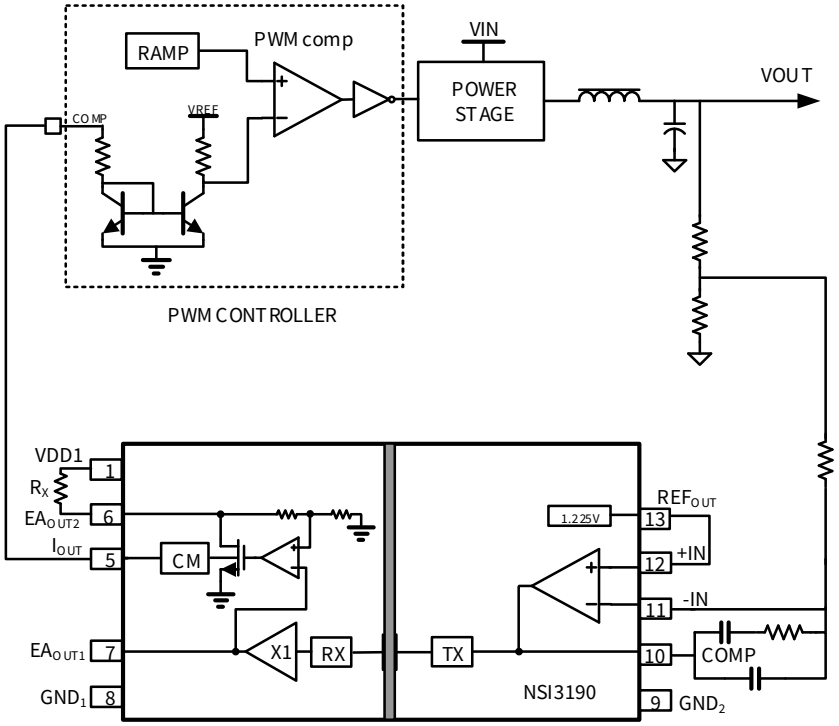


Figure 7.1 Current Output Application Diagram

7.2. Typical application circuit for E_{aout2} output

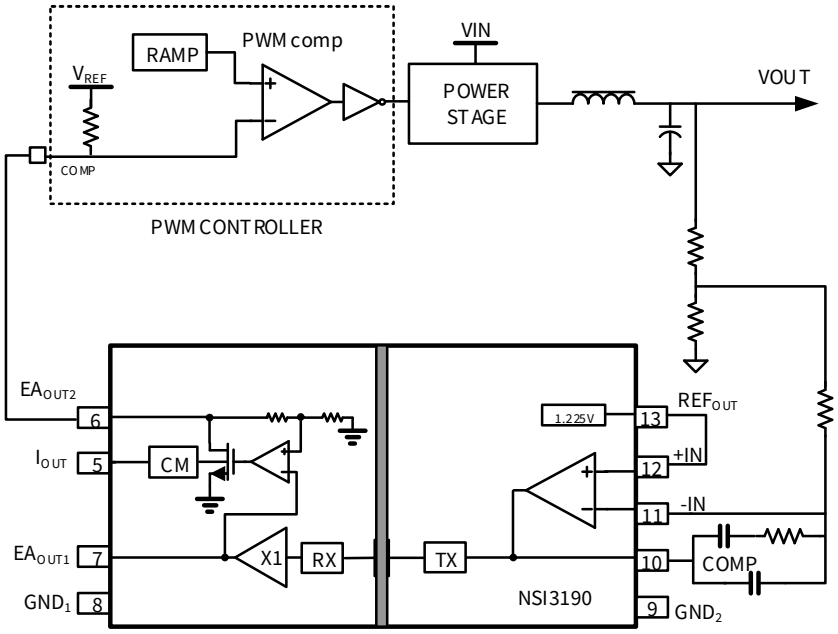


Figure 7.2 E_{aout2} Output Application Diagram

7.3. Typical test circuit

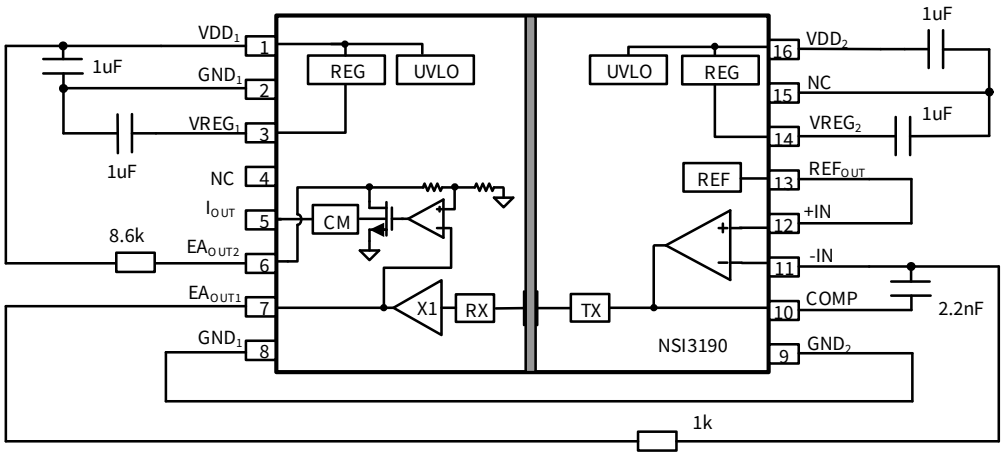


Figure 7.3 EA_{OUT1} accuracy test circuit

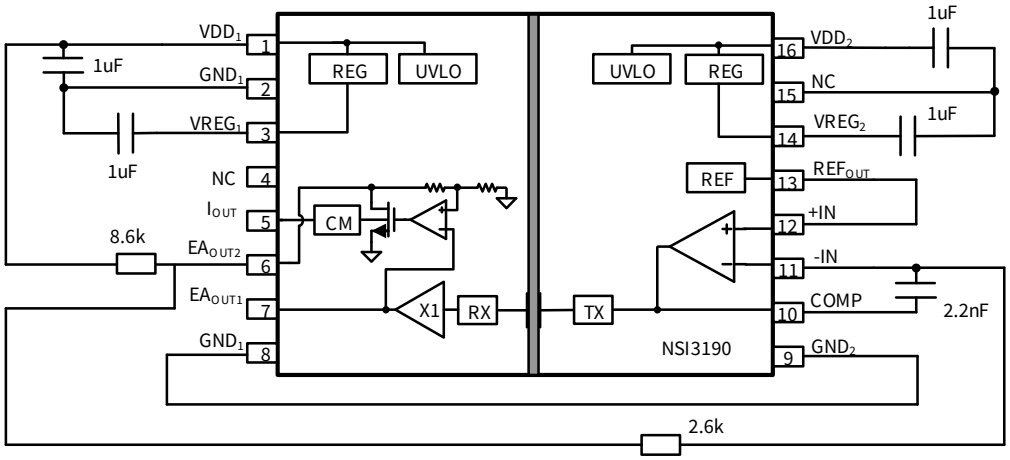


Figure 7.4 EA_{OUT2} accuracy test circuit

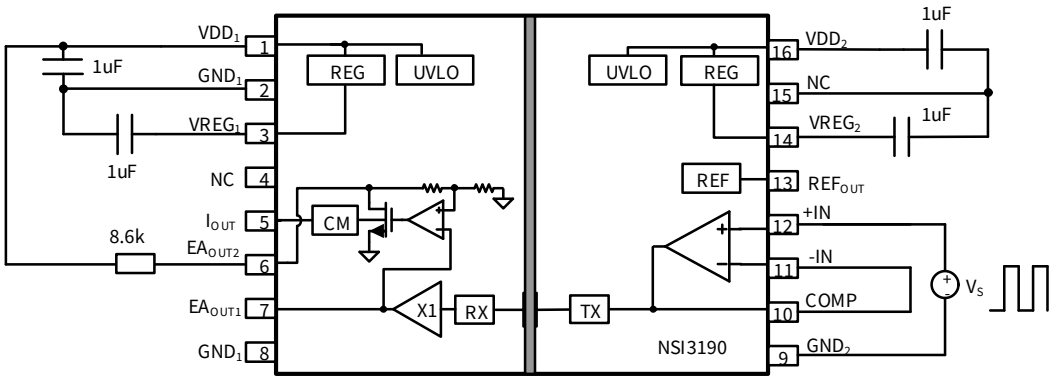


Figure 7.5 Signal following test circuit

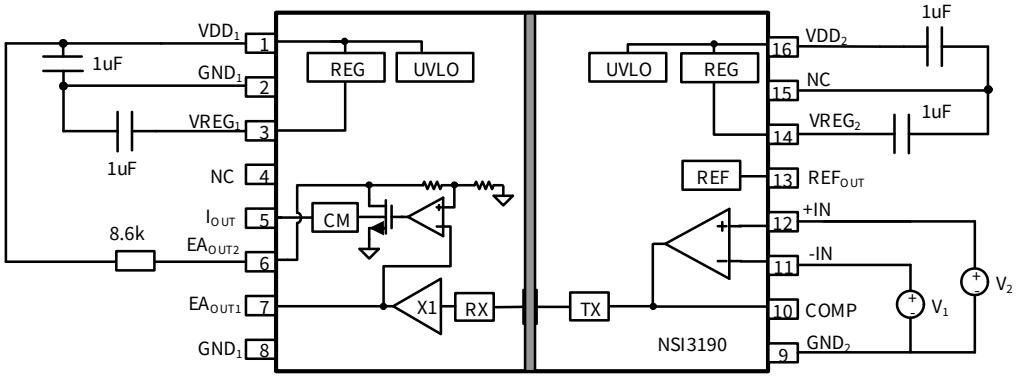


Figure 7.6 Test circuit of V_{OL}\V_{OH}

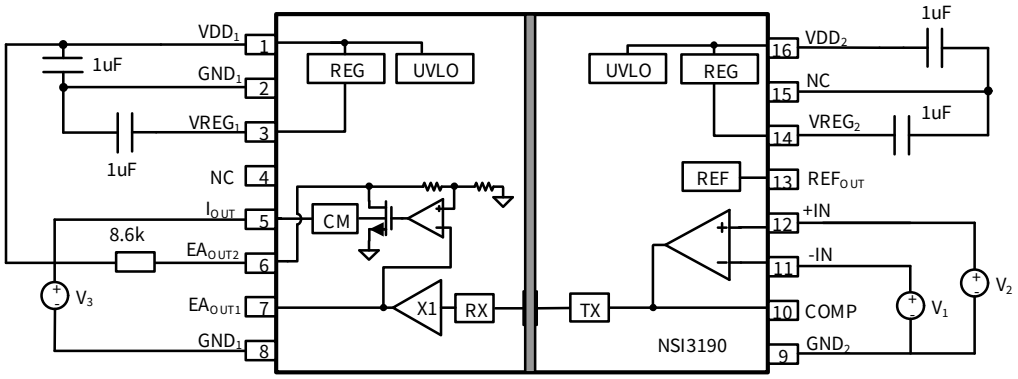


Figure 7.7 Test circuit of I_{OUTH}\I_{OUTL}

8. Package Information

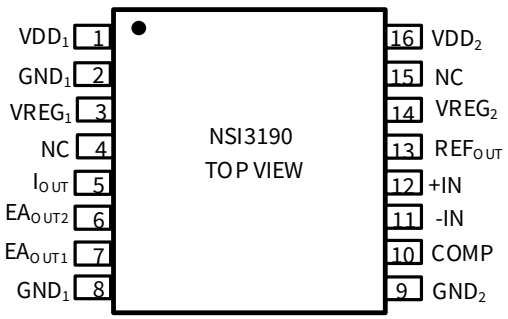
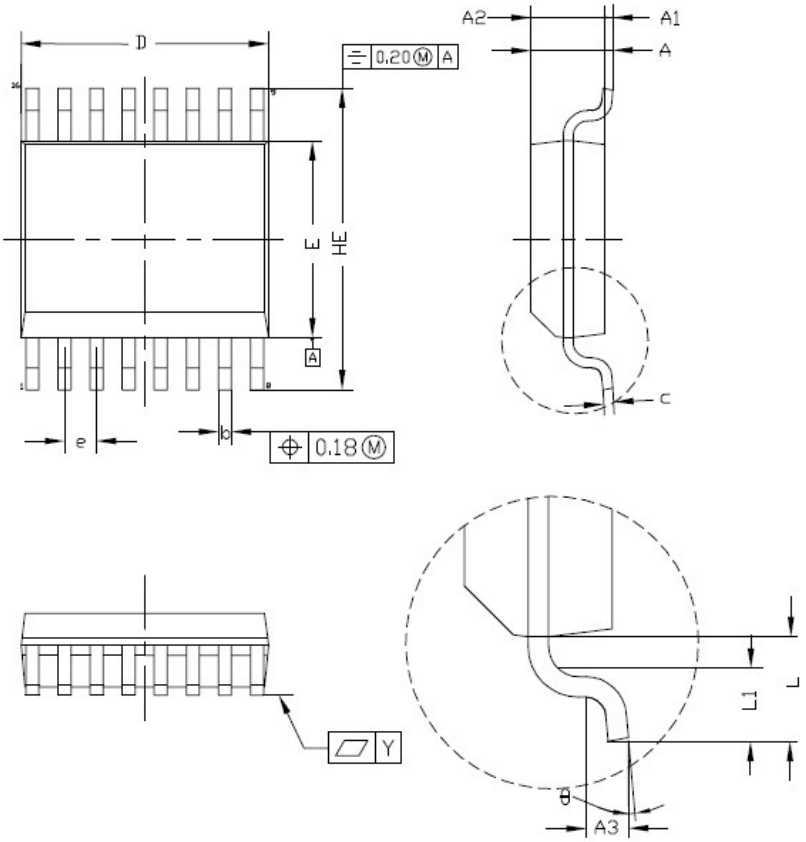


Figure 8.1. NSI3190 Package



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 8.2 SSOP16 Package Shape and Dimension in millimeters and (inches)

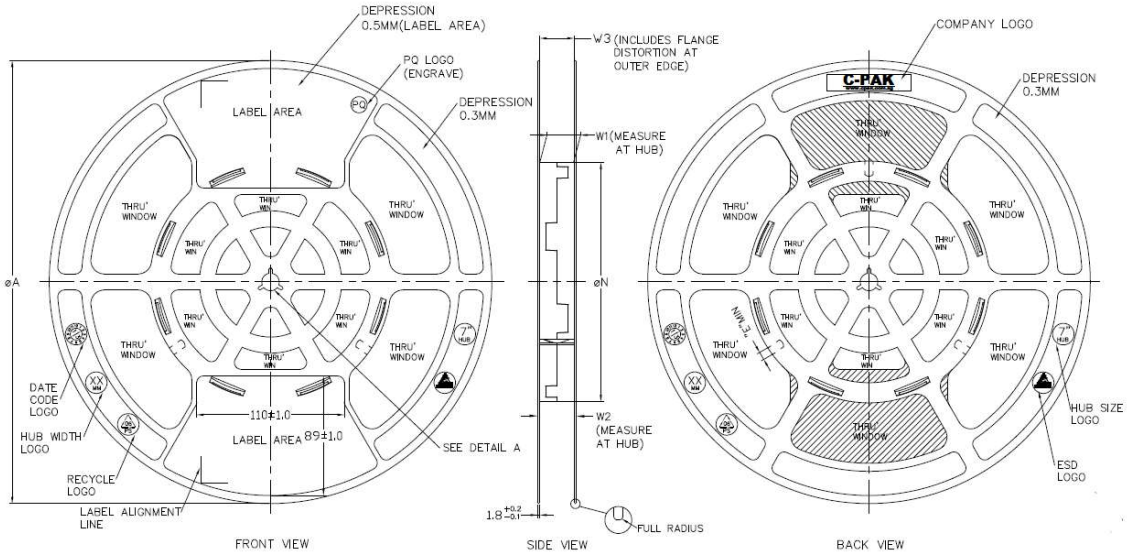
9. Ordering Information

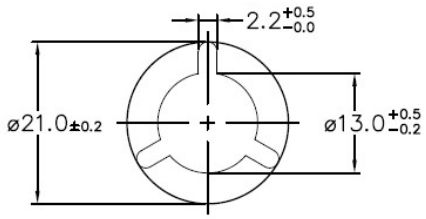
Part Number	*Isolation Rating (kV)*	*Default Output State*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSI3190-DSSR	3	Low	-40 to 125℃	1	SSOP16	SSOP16	2500

10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
Nsi3190	Click here	Click here	Click here	Click here

11. Tape and Reel Information

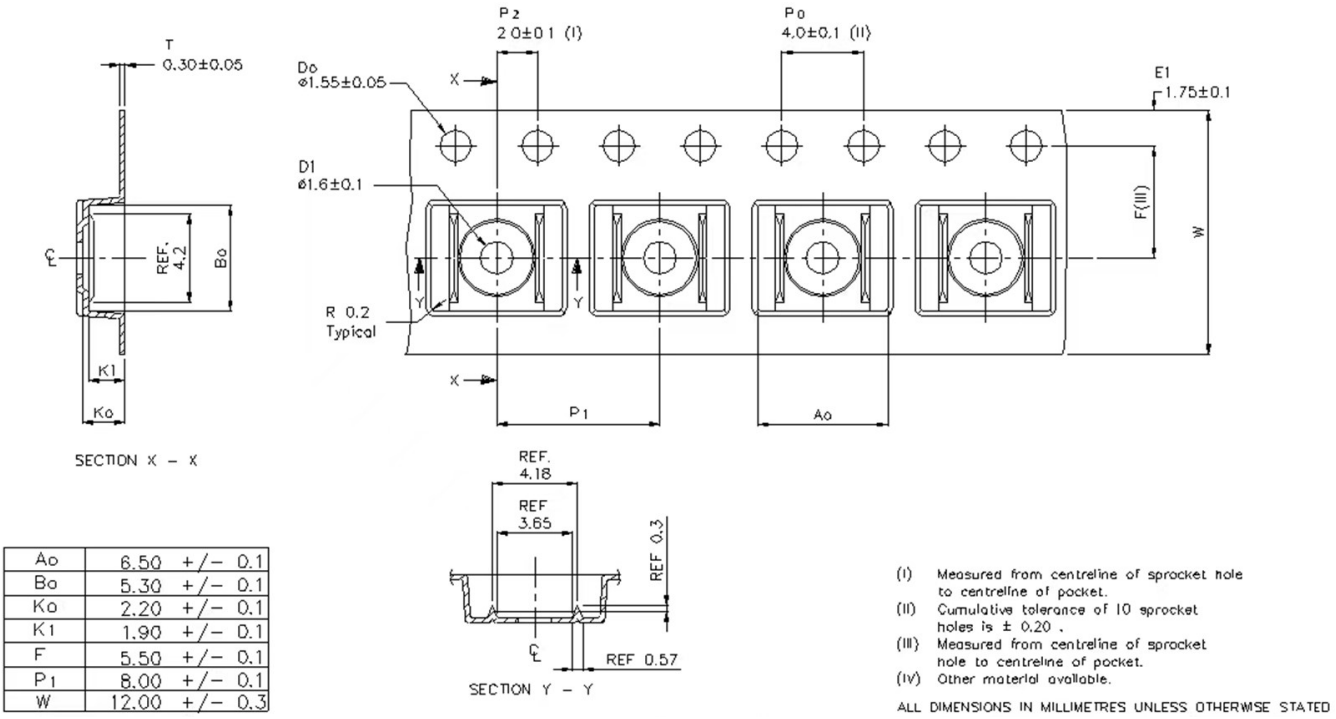




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 11.1 Tape and Reel Information of SSOP16

12. Revision History

Revision	Description	Date
1.0	Original	2020/2/16
1.1	Add min spec of BW_{OUTPUT}	2020/6/18
1.2	New format updated	2020/07/27
1.3	Delete maximum voltage of PGIN and PGOUT in part 2, Figure 4.11 Response delay PGIN to PGOUT and Figure 4.12 Response delay PGIN to +IN. Update the definition of pin 15 in part 1, the standard on which V_{IOSM} test method is based in 5.2, Regulatory Information in 5.3, tape and reel information in Figure 11.1 and important notice at the end of the datasheet. Update typeface to Source Sans Pro.	2023/01/11

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